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SUBJECT: MAGIC I Logic

ABSTRACT

The logical equations and a descriptive glossary of logical terms for
the MAGIC I computer is presented

Attached is a copy of the revised logical equations for the MAGIC I
computer, together with a descriptive glossary of all logical terms.

Due to the prototype nature of the computer, logical changes are to be
expected. Changes contemplated for the MAGIC II computer will first be made in
MAGIC I, wherever possible, to verify their logical correctness. When changes are
made, revised copies of the affected pages will be forwarded to the above distribution.

*Original Instruction Processing Unit Logic by F. Gurzi.

1. INSTRUCTION PROCESSING UNIT

1.1. CORE MEMORY READ AND CONTROL

1.1.1. READ AND RESTORE

$$MROS = SAO\ CPS \qquad\qquad ODD\ BITS$$
$$MROR = SAO^*\ CPS$$

$$MRES = SAE\ CPS \qquad\qquad EVEN\ BITS$$
$$MRER = SAE^*\ CPS$$

$$CMO = MRO(TRS\ CZ + STO)^* + M1\ TRS\ CZ + A1\ STO$$

$$CME = MRE(TRS\ CZ + STO)^* + M2\ TRS\ CZ + A2\ STO$$

1.1.2. SERIAL OUTPUT

$$CMS = CMO\ ODT + CME\ EDT$$

1.1.3. READ/WRITE CONTROL

$$RDIS = [(MPY + DIV)PO6 + IDL\ WS^*]\ DT24$$
$$RDIR = [(MPY + DIV)CZ + EX + WS\ ]\ DT24$$

$$WDIS = RDI\ DT1$$
$$WDIR = RDI^*\ DT1$$

1.2. INSTRUCTION BUFFER REGISTER

$$IB24PS = CMS(C2\ IDL^*\ EX^* + TP6)$$
$$\qquad\quad + IB1[C2^*(DY^* + CZ) + IDL\ EX^*]$$
$$\qquad\quad + ENTKYS\ EX$$
$$IB24PR = IB24PS^*$$

$$IB24S = IB24P\ CP^*$$

$$IB24R = IB24P^*\ CP^*$$

$$IBnPS = IBn+1 \qquad n = 23,22,\ldots\ldots 1$$
$$IBnPR = IBn+1^*$$

$$IBnS = IBnP\ CP^*$$
$$IBnR = IBnP^*\ CP^*$$

$$IBGC = (C2 + TP6)CP5 + (C1\ DT2-7 + C2^*\ DT1223)(DY^* + CZ)CP1$$

1.3. OPERATION CODE REGISTER

OR6S = IB24	STO = OR6*	OR5*	OR4*	OR3	C2*	
OR6R = IB24*	ADD = OR6*	OR5*	OR4	OR3*	C2*	
	SUB = OR6*	OR5*	OR4	OR3	C2*	
OR5S = IB23	LDA = OR6*	OR5	OR4*	OR3*	C2*	
OR5R = IB23*	MSK = OR6*	OR5	OR4*	OR3	C2*	
	DIV = OR6*	OR5	OR4	OR3*	C2*	
OR4S = IB22	MPY = OR6*	OR5	OR4	OR3	C2*	
OR4R = IB22*						
	TRA = OR6	OR5*	OR4*	OR3	C2*	
OR3S = IB21 + TRM	TRS = OR6	OR5*	OR4	OR3*	C2*	
OR3R = IB21* TRM*						

OR2S = IB20	LPS = OR6	OR5	OR4*	OR3*	OR2*	OR1*	C2*
OR2R = IB20*	RTE = OR6	OR5	OR4*	OR3*	OR2*	OR1	C2*
	XAB = OR6	OR5	OR4*	OR3*	OR2	OR1*	C2*
OR1S = IB19	SBR = OR6	OR5	OR4*	OR3*	OR2	OR1	C2*
OR1R = IB19*	MBR = OR6	OR5	OR4*	OR3	OR2*	OR1*	C2*
ORGC = BC CP*	INP = OR6	OR5	OR4	OR3*	OR2*	OR1*	C2*
	OUT = OR6	OR5	OR4	OR3*	OR2*	OR1	C2*
TRM = IB24 IB23* IB22* A24	DSI = OR6	OR5	OR4	OR3*	OR2	OR1*	C2*
	DSO = OR6	OR5	OR4	OR3*	OR2	OR1	C2*
BCS = SE CP5	JMP = OR6	OR5	OR4	OR3	A24	C2*	
BCR = DT1 CP5							

DY = TRA + TRS + MPY + DIV

C2 = DIV P2 + MPY PC3 + (TRA + TRS)PC5

1.4. CONTROL COUNTER AND INPUT/OUTPUT ADDRESS REGISTER

$$CA1PS = CA1^* \ DEC + (IB14 + MDTN)SE \qquad\qquad CA1S = CA1P \ CP^*$$
$$CA1PR = CA1PS^* \qquad\qquad\qquad\qquad\qquad\qquad\qquad CA1R = CA1P^* \ CP^*$$

$$CA2PS = CA2^* \ CA1^* \ DEC + (IB15 + MDTN)SE \qquad CA2S = CA2P \ CP^*$$
$$CA2PR = CA2 \ CA1^* \ DEC + IB15^* \ MDTN^* \ SE \qquad CA2R = CA2P^* \ CP^*$$

$$CA3PS = PZ \ DEC + (IB16 + MDTN)SE \qquad\qquad CA3S = CA3P \ CP^*$$
$$CA3PR = PC4 \ DEC + IB16^* \ MDTN^* \ SE \qquad\qquad CA3R = CA3P^* \ CP^*$$

$$CA4PS = CA4^* \ PZ \ DEC + IB17 \ SE \qquad\qquad\quad CA4S = CA4P \ CP^*$$
$$CA4PR = CA4 \ PZ \ DEC + IB17^* \ SE \qquad\qquad\quad CA4R = CA4P^* \ CP^*$$

$$CA5PS = IB18 \ SE \qquad\qquad\qquad\qquad\qquad\qquad CA5S = CA5P \ CP^*$$
$$CA5PR = CA4^* \ PZ \ DEC + IB18^* \ SE \qquad\qquad\quad CA5R = CA5P^* \ CP^*$$

$$CA6PS = IB13 \ SE \qquad\qquad\qquad\qquad\qquad\qquad CA6S = CA6P \ CP^*$$
$$CA6PR = IB13^* \ SE \qquad\qquad\qquad\qquad\qquad\quad CA6R = CA6P^* \ CP^*$$

$$CAGC = C2^* \ DT24 \ CP5 + (LRS + RTE)DT24^* \ CP1$$

$$DEC = DY \ CZ^* + SCS$$

$$MDTN = IB24^* \ IB23 \ IB22 + IB24 \ IB23^* + JN$$

$$JN = IB24 \ IB22 \ IB21$$

$$SE = (DY^* + CZ)DT24 \ C2^*$$

$PC7 = CA3 \ CA2 \ CA1$			$SC7$		
$PC6 = CA3 \ CA2 \ CA1^*$			$SC6$	(Not decoded)	
$PC5 = CA3 \ CA2^* \ CA1$			$SC5$		
$PC4 = CA3 \ CA2^* \ CA1^*$			$SC4 = CA6 \ CA5^* \ CA4^*$		
$PC3 = CA3^* \ CA2 \ CA1$			$SC3 = CA6^* \ CA5 \ CA4$		
$PC2 = CA3^* \ CA2 \ CA1^*$			$SC2 = CA6^* \ CA5 \ CA4^*$		
$PC1 = CA3^* \ CA2^* \ CA1$			$SC1 = CA6^* \ CA5^* \ CA4$		
$PZ = CA3^* \ CA2^* \ CA1^*$			$SZ = CA6^* \ CA5^* \ CA4^*$		

1.4.1. LRS AND RTE CONTROL

$$SCFPS = CA6 \ DT24 \ CP1 \qquad\qquad\qquad SCFS = SCFP \ CP^*$$
$$SCFPR = DT1 \qquad\qquad\qquad\qquad\qquad\quad SCFR = SCFP^* \ CP^*$$

$$SCS = (PZ^* + CA4 + CA5)(LRS + RTE)DT1-12$$

$$SCP = CA6(LRS + RTE)DT1-12^*$$

1.5. OPERATION CYCLE COUNTER

$$C1PS = C0(DY^* + CZ)$$
$$C1PR = C1(DY^* + CZ) + TP6$$

$$C1S = C1P \; CP^*$$
$$C1R = C1P^* \; CP^*$$

$$C2PS = C1(DY^* + CZ)$$
$$C2PR = C2(DY^* + CZ)IDL^*$$

$$C2S = C2P \; CP^*$$
$$C2R = C2P^* \; CP^*$$

$$CGC = DT24 \; CP5$$

$$C0 = C1^* \; C2^*$$

1.6. INSTRUCTION COUNTER

$$IC12PS = IC1(TP7^* \; DZ1^* \; C2^* + TP7 \; DT1823 + IDL)$$
$$+ CMS \; TP7 \; DT1\text{-}12$$
$$+ S4 \; DZ1$$
$$+ AB1 \; C2(INT1^* + INT2)IDL^*$$
$$+ M2 \; C2 \; INT1 \; INT2^* \; IDL^*$$
$$IC12PR = IC12PS^*$$

$$IC12S = IC12P \; CP^*$$

$$IC12R = IC12P^* \; CP^*$$

$$ICnPS = ICn+1 \qquad n = 11,10,\ldots\ldots,1$$
$$ICnPR = ICn+1^*$$

$$ICnS = ICnP \; CP^*$$
$$ICnR = ICnP^* \; CP^*$$

$$ICGC = (TP7^* \; DT1217 + TP7 \; DT1823)CP1 + TP7 \; DT1\text{-}12 \; CP5$$

$$TP6 = (TRA + TRS)PC6$$

$$TP7 = (TRA + TRS)PC7$$

$$DZ1 = (DY^* + CZ)C1$$

1.6.1. INSTRUCTION COUNT INCREMENTER

$$S3 = IC1 \oplus CY3$$

$$CY3PS = DZ1 \; JMP^* \; IDL^* \; DT11 \; CP1$$
$$CY3PR = (IC1^* \; DT11^* + DT18) \; CP1$$

$$CY3S = CY3P \; CP^*$$
$$CY3R = CY3P^* \; CP^*$$

1.7. BIAS REGISTER

$$BR12PS = (BR1 \; MBR^* + AB1 \; MBR)TP7^*(SBR^* + DT1823)$$
$$+ CMS \; TP7$$
$$+ AB1 \; SBR \; DT1214$$
$$BR12PR = BR12PS^*$$

$$BR12S = BR12P \; CP^*$$

$$BR12R = BR12P^* \; CP^*$$

$$BRnPS = BRn+1 \qquad n = 11,10,\ldots\ldots,1$$
$$BRnPR = BRn+1^*$$

$$BRnS = BRnP \; CP^*$$
$$BRnR = BRnP^* \; CP^*$$

$$BRGC = TP7^* \; DT1217 \; CP1 + (TP7 + SBR \; DT1823)DT1\text{-}12^* \; CP5$$

1.7.1. BIAS REGISTER AND INSTRUCTION COUNTER ODD/EVEN OUTPUT

$$BDOS = BR1 \; DT1-12^* + ICl \; DT1-12$$
$$BDOR = BDOS^*$$
$$BDOC = CP7$$

$$BDT = BDOS$$

1.8. OPERAND ADDRESS ADDER

$$S4 = X4 \oplus Y4 \oplus CY4$$

$$X4 = IB13(X4G + JC)DT1217 + CC$$

$$Y4 = (BR1 \; BIS^* + ICl \; BIS)Y4G \; DT1217$$

$$X4GS = (DY^* + CZ)DT10$$
$$X4GR = AC^* \; TC^* \; DT15 + DT16$$

$$Y4GS = (IB24^* \; IB20^* + IB24 \; IB23 \; IB21)(DY^* + CZ)DT10$$
$$Y4GR = DT18$$

$$CY4PS = X4 \; Y4 + INT1 \; TRS \; PC6 \; DT17 \qquad CY4S = CY4P \; CP^*$$
$$CY4PR = X4^* \; Y4^* \; CY4 \qquad\qquad\qquad\quad CY4R = CY4P^* \; CP^*$$
$$CY4GC = INT1 \; TRS \; PC6 \; DT17 \; CP5 + (INT1 \; TRS \; PC6 \; DT17)^*CP1$$

$$CCPS = (X4G \; AC^* \; TC^* \; JC^* \; IB13 \; DT14 + AC \; DT15)CP5 \qquad CCS = CCP \; CP^*$$
$$CCPR = DT17 \; CP5 \qquad\qquad\qquad\qquad\qquad\qquad\qquad CCR = CCP^* \; CP^*$$

$$ACS = IB24^* \; IB20(DY^* + CZ)DT10$$
$$ACR = DT17$$

$$TCS = IB24 \; IB23^*(DY^* + CZ)DT10$$
$$TCR = DT17$$

$$JS = JN \; IB23(DY^* + CZ)DT10$$
$$JCR = IB12^* \; DT16 + DT18$$

$$BISS = (JN + IB19)DT10$$
$$BISR = JN^* \; IB19^* \; DT10$$

1.9. MEMORY ADDRESS BUFFER REGISTER

$$AB12PS = I\,C1(C2\ IDL^* + TP7)$$
$$+ S3\ DT1(INT1^* + INT)$$
$$+ S4\ [CO(DY^* + CZ) + TRS\ PC6]$$
$$+ AB1\ IDL\ EN^*$$
$$+ ENTKYS\ EN$$
$$+ INT1\ INT$$

$$AB12PR = AB12PS^*$$

$$ABnPS = ABn+1 \qquad n = 11,10,......,1$$
$$ABnPR = ABn+1^*$$

$$ABGC = [(DY^*\ JMP^* + CZ)DT1217 + (INT1\ INT + TRS\ PC6 + TP7)DT1823]\ EN^*\ CP1$$
$$+ DT1\text{-}12\ EN\ CP5$$

$$AB12S = AB12P\ CP^*$$

$$AB12R = AB12P^*\ CP^*$$

$$ABnS = ABnP\ CP^*$$
$$ABnR = ABnP^*\ CP^*$$

1.10. MEMORY ADDRESS REGISTER

$$MAnS = ABn \qquad n = 12,11,......,1$$
$$MAnR = ABn^*$$

$$MAGC = DT24\ CP6$$

1.11. INTERRUPT

$$INT1S = INT3(MDTN^* + CZ)(IB12^* + IB11)C1\ DT1\ CP7$$
$$INT1R = TRS\ CZ + INT2\ TRS^*\ CO\ CP1$$

$$INT2S = INT1\ INT^*\ C1$$
$$INT2R = INT1^*$$

$$INT3S = INT\ INT1^*\ DT24$$
$$INT3R = INT2$$

$$INT4S = C2\ INT1$$
$$INT4R = FC3P\ DT24$$

$$INT5S = MCUINT$$
$$INT5R = INT4$$

$$INT = FC4P\ FC1P\ GF\ INT4^*\ NORMINT\ IDL^* + INT5$$

1.12. IDLE

IDLS = LOGIDL EX* WS* C2 DT1
IDLR = (LOGIDL* + EX + WS)C2 DT1

1.13. MCU INPUT SYNC.

EXS = EXINST IDL
EXR = IDL* CO DT1

WSS = WDSTEP IDL
WSR = IDL* CO DT1

ENS = ENTCTR IDL DT1
ENR = DT18

2. ARITHMETIC UNIT

2.1. ACCUMULATOR REGISTER

A24PS = S2(W24 + W27 + ADD + SUB)
    + S1 W25
    + B1 SCP LHS
    + B2(DIV CZ DT24* + XAB + SCP SCP* + RTE)
    + MRE(A2 MSK + LDA)
    + IE INP
    + ID DSI DT24
    + A2(DIV PC7 + STO + OUT + DSI DT24 + IDL)
    + A24 LRS DT1-12

A24PR = A24PS*

A23PS = S1(W24 + W27 + ADD + SUB)
    + S2D W25
    + B1(DIV CZ + XAB + SCP + RTE)
    + MRO(A1 MSK + LDA)
    + IO INP
    + A1(DIV PC7 + STO + OUT + DSI + IDL)
    + A24 LRS DT1-12

A23PR = A23PS*

AnPS = An+2   n = 22,21,........,1
AnPR = An+2

ABPS = B1 DIV PC7
    + A2(W27 LBT* + DIV*)
    + BB W27 LBT
ABPR = ABPS*

Right column:

A24S = A24P CP*

A24R = A24P* CP*

A23S = A23P CP*

A23R = A23P* CP*

AnS = AnP CP*
AnR = AnP* CP*

ABS = ABP CP*

ABR = ABP* CP*

AGC = BGC + (LDA + ADD + SUB + STO + INP + OUT + MSK + DSI + IDL)CP3

ARS = A1 ODT + A2 KDT

2.2. MULTIPLIER/QUOTIENT REGISTER

$$B24PS = A2(MPY\ PC7 + W24\ LBT + DIV\ CZ + XAB)$$
$$+ B2(MPY\ PC7^* \ LBT^* + DIV\ PC7 + RTE)$$
$$+ B1\ MPY\ CZ\ LBT$$
$$+ B1(W27 + LRS\ SCP)$$
$$+ A24\ LRS\ SCP^*$$
$$B24PR = B24PS^*$$

$B24S = B24P\ CP^*$

$B24R = B24P^*\ CP^*$

$$B23PS = A1(MPY\ PC7 + W24\ LBT + DIV\ CZ + XAB)$$
$$+ B1(MPY\ PC7^*\ LBT^* + DIV\ PC7)$$
$$+ A2(MPY\ CZ\ LBT + RTE + LRS)$$
$$+ DC\ W27\ FBT^*$$
$$B23PR = B23PS^*$$

$B23S = B23P\ CP^*$

$B23R = B23P^*\ CP^*$

$$B22PS = A1(LRS + RTE) + B24\ LRS^*\ RTE^*$$
$$B22PR = B22PS^*$$

$B22S = B22P\ CP^*$

$B22R = B22P^*\ CP^*$

$$BnPS = Bn+2 \qquad n = 21, 20, \ldots\ldots, 1$$
$$BnPR = Bn+2^*$$

$BnS = BnP\ CP^*$

$BnR = BnP^*\ CP^*$

$$BBPS = B2$$
$$BBPR = B2^*$$

$BBS = BBP\ CP^*$

$BBR = BBP^*\ CP^*$

$$BGC = (W24 + W25 + W27 + SCS + SCP)CP1$$
$$+ (MPY\ PC7 + DIV\ W27^* + XAB)CP3$$

2.3. MULTIPLICAND/DIVISOR REGISTER

$$M24PS = [LRE(MPY + DIV) + BIE\ TRS]\ PC7$$
$$+ (MB\ MPY + M2\ DIV)CZ^*\ PC7$$
$$+ ICL\ INT\ INT1$$
$$M24PR = M24PS^*$$

$M24S = M24P\ CP^*$

$M24R = M24P^*\ CP^*$

$$M23PS = [LRO(MPY + DIV) + BIO\ TRS]\ PC7$$
$$+ (MA\ MPY + M1\ DIV)PC7^*$$
$$M23PR = M23PS^*$$

$M23S = M23P\ CP^*$

$M23R = M23P^*\ CP^*$

$$MnPS = Mn+2 \qquad n = 22, 21, \ldots\ldots, 1$$
$$MnPR = Mn+2^*$$

$MnS = MnP\ CP^*$

$MnR = MnP^*\ CP^*$

$$MBPS = M2(MPY^* + PC7^*)$$
$$MBPR = MBPS^*$$

$MBS = MBP\ CP^*$

$MBR = MBP^*\ CP^*$

$$MAPS = M1(MPY^* + PC7^*)$$
$$MAPR = MAPS^*$$

$MAS = MAP\ CP^*$

$MAR = MAP^*\ CP^*$

$$MGC = [(W24 + W25 + W27 + SCS + SCP)LRS^*\ RTE^*\ PC7^* + MCK]\ IDL^*\ CP1$$
$$+ [(MPY + DIV)PC7 + TRS(PC7 + PC5)]\ CP3$$

$$MCK = INT1\ INT2^*\ CO^*\ DT1217^*$$

2.4. MULTIPLY CONTROL

<div style="display:flex; justify-content:space-between;">

$$D3PS = B4$$
$$D3PR = B4^*$$

$$D3S = D3P\ CP^*$$
$$D3R = D3P^*\ CP^*$$

$$D2PS = B4^*\ B3\ B2A + B4\ B3^*\ B2A^*$$
$$D2PR = D2PS^*$$

$$D2S = D2P\ CP^*$$
$$D2R = D2P^*\ CP^*$$

$$D1PS = B3\ B2A^* + B3^*\ B2A$$
$$D1PR = D1PS^*$$

$$D1S = D1P\ CP^*$$
$$D1R = D1P^*\ CP^*$$

</div>

$$DCC = G1\ CP1$$

$$G1 = (MPY + DIV)PC7^*\ LBT + (MPY^*\ DIV^* + PC7)DT24$$

$$W24S = MPY\ PC6\ DT1$$
$$W24R = DT24\ FBT$$

$$W25S = MPY\ PC4\ DT24\ FBT$$
$$W25R = DT7$$

2.5. DIVIDE CONTROL

$$DCPS = (A2 \oplus DDE^*)PC7 + (A1 \oplus CY2)PC7^*$$
$$DCPR = DCPS^*$$

$$DCS = DCP\ CP^*$$
$$DCR = DCP^*\ CP^*$$

$$DCCC = G1\ CP1$$

$$W27S = DIV\ PC6\ DT1$$
$$W27R = (CC + IDL)DT1$$

2.6. ADDERS

$$S1 = X1 \oplus Y1 \oplus CY1$$

$$X1 = A1\ G2 + AB\ G2^*$$

$$Y1 = M1\ G3 + MB(D1\ LBT + D2)MPY + MRO\ MPY^*\ DIV^*$$

$$CY1PS = [(Y2 + CY2)(X2 \oplus AD^*) + Y2\ CY2]\ G1^*$$
$$CY1PR = CY1PS^*$$

$$CY1S = CY1P\ CP^*$$
$$CY1R = CY1P^*\ CP^*$$

$$CY1CC = (MPY + DIV)CP1 + MPY^*\ DIV^*\ CP3$$

$$S2 = (X2 \oplus Y2 \oplus CY2)(MPY^* + PC7^*)$$

$$X2 = A2\ G2 + A1\ DIV + AB\ LBT\ MPY$$

$$Y2 = M2\ G3 + M1\ D2\ LBT^*\ MPY + MB(D1 + D2)LBT\ MPY + MRE\ MPY^*\ DIV^*$$

$$CY2 = (Y1 + CY1)(X1 \oplus AD^*) + Y1\ CY1$$

$$G2 = LBT^*\ MPY + MPY^*\ DIV^*$$

$$G3 = D1\ LBT^*\ MPY + DIV$$

$$S2D2S = S2\ AGC$$
$$S2DR = S2^*\ AGC$$

$$S2DS = S2DP\ CP^*$$
$$S2DR = S2DP^*\ CP^*$$

$$AD^* = D3\ MPY + DC\ DIV + SUB$$

2.7. MULTIPLY/DIVIDE BIT COUNTER

$$MC1PS = MC1^* \ MC4^*(MC3 + MC2^*) + MC3^* \ MC4 \ DIV$$
$$MC1PR = MC1(MC4^* + MC2 \ MC3)$$

$$MCnPS = MCn\text{-}1 \qquad\qquad n = 2,3,\dots,6$$
$$MCnPR = MCn\text{-}1^*$$

$$MCGC = -(PC7^* + FBT^*)CP1$$

$$FBT = MC1 \ MC2^* \ MC3^* \ MC4$$
$$LBT = MC2^* \ MC3 \ MC4^*$$

$$MC1S = MC1P \ CP^*$$
$$MC1R = MC1P^* \ CP^*$$

$$MCnS = MCnP \ CP^*$$
$$MCnR = MCnP^* \ CP^*$$

2.8. DISCRETE INPUTS

$$
\begin{aligned}
ID = \ & FLY \ SZ \ \ PC3 + IAA \ SZ \ \ PC4 + ICP \ SZ \ \ PC5 + MCD \ SZ \ \ PC6 + NAV \ SZ \ \ PC7 \\
& EXO \ SC1 \ PC3 + S01 \ SC1 \ PC4 + S02 \ SC1 \ PC5 + S03 \ SC1 \ PC6 + S04 \ SC1 \ PC7 \\
& S05 \ SC2 \ PC3 + S06 \ SC2 \ PC4 + S07 \ SC2 \ PC5 + S10 \ SC2 \ PC6 + DER \ SC2 \ PC7 \\
& SSP\text{-}SC3 \ PC3 + TAR \ SC3 \ PC4 + TIM \ SC3 \ PC5 + TSA \ SC3 \ PC6 + TSB \ SC3 \ PC7
\end{aligned}
$$

3. ACCELEROMETER AND OUTPUT PROCESSING UNITS (APU, OPU)

3.1. ACCELEROMETERS AND REAL TIME

3.1.1. ACCELEROMETER PROCESSING

3.1.1.1. U AXIS

$AUR1S = IUR$ DT23 CP5
$AUR2R = IUR^*$ DT23 CP5

$AUR2S = AUR1$ DT24 CP5
$AUR2R = AUR1^*$ DT24 CP5

$AUQ1S = IUQ$ DT23 CP5
$AUQ1R = IUQ^*$ DT23 CP5

$AUQ2S = AUQ1$ DT24 CP5
$AUQ2R = AUQ1^*$ DT24 CP5

$AUBS = [AUR1^* (AUQ1\ AUQ2^* + AUQ1^*\ AUR2)$
$\quad + AUR1\ (AUQ1^*\ AUR2^* + AUQ1^*\ AUC2]\ DT24\ CP^*$
$AUBR = DT6\ IUV^*\ CP^*$

$AUCS = [AUR1^* (AUQ1^*\ AUQ2 + AUQ1\ AUR2)$
$\quad + AUR1\ (AUC1^*\ AUR2^* + AUQ1\ AUC2^*]\ DT24\ CP^*$
$AUCR = DT6\ IUV^*\ CP^*$

3.1.1.2. V AXIS

$AVR1S = IVR$ DT5 CP5
$AVR1R = IVR^*$ DT5 CP5

$AVR2S = AVR1$ DT6 CP5
$AVR2R = AVR1^*$ DT6 CP5

$AVQ1S = IVQ$ DT5 CP5
$AVQ1R = IVQ^*$ DT5 CP5

$AVQ2S = AVQ1$ DT6 CP5
$AVQ2R = AVQ1^*$ DT6 CP5

$AVBS = [AVR1^* (AVQ1\ AVQ2^* + AVQ1^*\ AVQ2)$
$\quad + AVR1\ (AVQ1\ AVR2^* + AVQ1^*\ AVQ2]\ DT6\ CP^*$
$AVBR = DT12\ IUV^*\ CP^*$

$AVCS = [AVR1^* (AVQ1^*\ AVQ2 + AVQ1\ AVR2)$
$\quad + AVR1\ (AVQ1^*\ AVR2^* + AVQ1\ AVQ2^*]\ DT6\ CP^*$
$AVCR = DT12\ IUV^*\ CP^*$

3.1.1.3. W AXIS

$AWR1S = IWR$ DT11 CP5
$AWR1R = IWR^*$ DT11 CP5

$AWR2S = AWR1$ DT12 CP5
$AWR2R = AWR1^*$ DT12 CP5

$AWQ1S = IWQ$ DT11 CP5
$AWQ1R = IWQ^*$ DT11 CP5

$AWQ2S = AWQ1$ DT12 CP5
$AWQ2R = AWQ1^*$ DT12 CP5

$AWBS = [AWR1^* (AWQ1\ AWQ2^* + AWQ1^*\ AWR2)$
$\quad + AWR1\ (AWQ1\ AWR2^* + AWQ1^*\ AWQ2]\ DT12\ CP^*$
$AWBR = DT18\ IWD^*\ CP^*$

$AWCS = AWR1^* (AWQ1^*\ AWQ2 + AWQ1\ AWR2)$
$\quad + AWR1\ (AWQ1^*\ AWR2^* + AWQ1\ AWQ2^*]\ DT12\ CP^*$
$AWCR = DT18\ IWD^*\ CP^*$

3.1.2. ACCELEROMETER AND REAL TIME REGISTERS

3.1.2.1. U AND V ACCELEROMETER REGISTER

$$UV18PS = HAS\ IUV^*$$
$$UV18PR = UV18PS^*$$

$$UV18S = UV18P\ CP^*$$
$$UV18R = UV18P^*CP^*$$

$$UVnPS = UVn+1 \qquad n = 17,16,\ldots\ldots,1$$
$$UVnPR = UVn+1^*$$

$$UVnS = UVnP\ CP^*$$
$$UVnR = UVnP^*\ CP^*$$

$$UVGC = HAT^*\ DT1223^*\ IUV^*\ CP1 + (DT1-9 + DT1321)IUV\ CP5$$

$$IUV = INP\ PZ$$

3.1.2.2. W ACCELEROMETER AND DELTA T REGISTER

$$WD18PS = HAS\ IWD^*$$
$$WD18PR = WD18PS^*$$

$$WD18S = WD18P\ CP^*$$
$$WD18R = WD18P^*CP^*$$

$$WDnPS = WDn+1 \qquad n = 17,16,\ldots\ldots,1$$
$$WDnPR = WDn+1^*$$

$$WDnS = WDnP\ CP^*$$
$$WDnR = WDnP^*\ CP^*$$

$$WDGC = HAT^*\ DT1223\ IWD^*\ CP1 + (DT1-9 + DT1321)IWD\ CP5$$

$$IWD = INP\ PC1$$

$$HATPS = (DT5 + DT11 + DT17 + DT23)CP1$$
$$HATPR = (DT6 + DT12 + DT18 + DT24)CP5$$

$$HATS = HATP\ CP^*$$
$$HATR = HATP^*\ CP^*$$

3.1.2.3. SERIAL INPUTS TO A REGISTER

$$IADOS = (UV1\ IUV + WD1\ IWD)(DT1-9 + DT1321) + ASM\ DT1-9^*\ DT1321^*$$
$$IADOR = IADOS^*$$
$$IADOC = CP7$$

$$IADES = (UV2\ IUV + WD2\ IWD)(DT1-8 + DT1320) + ASM\ DT1-9^*\ DT1321^* + ASMS$$
$$IADER = IADES^*$$
$$IADEC = CP7$$

$$ASMS = [UV1\ IUV(DT9 - DT21) + WD1\ IWD\ DT9]\ CP7$$
$$ASMR = (DT1 + DT13)CP7$$

3.1.3. HALF ADDER A

$HAS = HAI \oplus HAK$

$HAI = UV1\ DT1223^* + WD1\ DT1223$

$HAKS = (HUK\ DT6-17^* + HVK\ DT6-17)DT1223^* + (HWK\ DT6-17 + HDK\ DT6-17^*)DT1223$
$HAKR = HAKS^*$
$HAKC = CP^*$

$HUKS = (AUB + AUC)HAT\ DT1223^*$
$HUKR = (UV1\ AUB + UV1^*\ AUC)HAT^* + DT1223$
$HUKC = CP1$

$HVKS = (AVB + AVC)HAT\ DT6-17$
$HVKR = (UV1\ AVB + UV1^*\ AVC)HAT^* + DT6-17$
$HVKC = CP1$

$HWKS = (AWB + AWC)HAT\ DT1223$
$HWKR = (WD1\ AWB + WD1^*\ AWC)HAT^* + DT1223^*$
$HWKC = CP1$

$HDKS = HAW\ HAT\ DT24^*$
$HDKR = (WD1^* , HAT^*\ DT6-17^*\ DT1223 + DT24)IWD^*$
$HDKC = CP1$

$HAWPS = HAW^*\ DT24\ CP5$ $HAWS = HAWP\ CP^*$
$HAWPR = HAW\ DT24\ CP5$ $HAWR = HAWP^*\ CP^*$

3.2. WORD COUNTER

$WC1PS = WC1^*\ DT24\ CP5$ $WC1S = (WC1P + ONS)DT1$
$WC1PR = WC1\ DT24\ CP5$ $WC1R = WC1P^*\ ONS^*\ DT1$

$WC2PS = WC2^*\ WC1P^*$ $WC2S = WC2P\ WC1P$
$WC2PR = WC2\ WC1P^*$ $WC2R = WC2P^*\ WC1P$

3.3. 400 CYCLE COUNTER

$$FC4PS = FC4^* \ FC1^*$$
$$FC4PR = FC4(FC2 + FC3^* \ FC1^*)$$

$$FC3PS = FC4$$
$$FC3PR = FC4^*$$

$$FC2PS = FC3$$
$$FC2PR = FC3^*$$

$$FC1PS = FC2$$
$$FC1PR = FC2^*$$

$$FC4S = FC4P \ CP1$$
$$FC4R = FC4P^* \ CP1$$

$$FC3S = FC3P \ CP1$$
$$FC3R = FC3P^* \ CP1$$

$$FC2S = FC2P \ CP1$$
$$FC2R = FC2P^* \ CP1$$

$$FC1S = FC1P \ CP1$$
$$FC1R = FC1P^* \ CP1$$

$$FCGC = GC1 \ CP^*$$

$$FOG = FRG + FC1P^* \ FC4P \ FC2P^*$$

$$FRG = FC1P(FC3P \ FC2P^* + FC3P^* \ FC2P)$$

3.4. GIMBAL ANGLE COUNTERS

3.4.1. GIMBAL ANGLE COUNT CONTROL

$$GC1S = GF^* \ GC2 \ CP1$$
$$GC1R = GC2 \ CP1$$

$$GC2S = GC1 \ CP^*$$
$$GC2R = GF \ CP^*$$

$$GC3S = GA^* \ FC4P^* \ FC2P \ FC1P^* \ GC1 \ GC2 \ CP$$
$$GC3R = FC2P^*$$

$$GC4PS = GCG \ CP1$$
$$GC4PR = GCG^* \ CP1$$

$$GC4S = GC4P \ CP^*$$
$$GC4R = GC4P^* \ CP^*$$

$$GCG = GF^* \ GSG + GC3(GF^* + GSG)$$

$$GSG = GA \ FC4P^* \ FC2P \ FC1P^* + FC4P \ FC3P(GB \ FC2P + GC \ FC2P^*)$$

3.4.2. GIMBAL ANGLE COUNTER - LOW ORDER

$GA1PS = (GA1^* \ GC4 + GRG)CP1$
$GA1PR = GA1 \ GC4 \ CP1$

$GA1S = GA1P \ CP^*$
$GA1R = GA1P^* \ CP^*$

$GA2PS = GA2^* \ GA1PR + GRG \ CP1$
$GA2PR = GA2 \ GA1PR$

$GA2S = GA2P \ CP^*$
$GA2R = GA2P^* \ CP^*$

$GA3PS = GA3^* \ GA2PR + GRG \ CP1$
$GA3PR = GA3 \ GA2PR$

$GA3S = GA3P \ CP^*$
$GA3R = GA3P^* \ CP^*$

$GA4PS = GA4^* \ GA3PR + GRG \ CP1$
$GA4PR = GA4 \ GA3PR$

$GA4S = GA4P \ CP^*$
$GA4R = GA4P^* \ CP^*$

$GA5PS = GA5^* \ GA4PR + GRG \ CP1$
$GA5PR = GA5 \ GA4PR$

$GA5S = GA5P \ CP^*$
$GA5R = GA5P^* \ CP^*$

$GA6PS = GA6^* \ GA5PR + GRG \ CP1$
$GA6PR = GA6 \ GA5PR$

$GA6S = GA6P \ CP^*$
$GA6R = GA6P^* \ CP^*$

$GA7PS = GA7^* \ GA6PR + GRG \ CP1$
$GA7PR = GA7 \ GA6PR$

$GA7S = GA7P \ CP^*$
$GA7R = GA7P^* \ CP^*$

$GC5S = GA7PR \ GC4 \ CP1$
$GC5R = GA7PR^* \ DT19^* \ CP1$

$GC6S = GC5 \ GA7PR^*$
$GC6R = GC5^* \ WC1 \ DT19$

$GRG = IGA \ DT24 + FRG$

$GAC = GC6 \ WC1 \ DT18$

3.4.3. GIMBAL ANGLE COUNTER - HIGH ORDER

$GA12PS = HBS + IGA + FRG$
$GA12PR = HBS^* \ IGA^* \ FRG^*$

$GA12S = GA12P \ CP^*$
$GA12R = GA12P^* \ CP^*$

$GAnPS = GAn+1$ $n = 11,10,9,8$
$GAnPR = GAn+1^*$

$GAnS = GAnP \ CP^*$
$GAnR = GAnP^* \ CP^*$

$GAGC = (WC1 + IGA + FRG)DT1923 \ CP5$

$IGA = INP \ PC3$

$GAE = GA1 \ DT11 + GA3 \ DT13 + GA5 \ DT15 + GA7 \ DT17 + GA9 \ DT1923$

$GAO = GA2 \ DT13 + GA4 \ DT15 + GA6 \ DT17 + GA8 \ DT1923$

$IGAES = GAE \ DT1121 \ CP7$
$IGAER = (GAE^* + DT1121^*)CP7$

$IGAOS = GAO \ DT1123 \ CP7$
$IGAOR = (GAO^* + DT1123^*)CP7$

3.5. EARTH NAVIGATION, STAR SCANNER AND EXTRAPOLATOR

3.5.1. EARTH NAV., STAR SCANNER AND EXTRAPOLATOR REGISTER

$$NS12PS = ARS \ ONS + HBS \ ONS^*(INS^* + DT1\text{-}12)$$
$$NS12PR = NS12PS^*$$

$$NS12S = NS12P \ CP^*$$
$$NS12R = NS12P^* \ CP^*$$

$$NSnPS = NSn{+}1 \qquad n = 11,10,\ldots\ldots,1$$
$$NSnPR = NSn{+}1^*$$

$$NSnS = NSnP \ CP^*$$
$$NSnR = NSnP^* \ CP^*$$

$$NSGC = [DT1\text{-}12^* \ INS + DT1\text{-}12(ONS + WC1)] \ CP5$$

$$INSES = NS2 \ DT1\text{-}12^* \ CP7$$
$$INSER = (NS2^* + DT1\text{-}12) CP7$$

$$INSOS = NS1 \ DT1\text{-}12^* \ CP7$$
$$INSOR = (NS1^* + DT1\text{-}12) CP7$$

$$INS = INP \ PC2$$

$$ONS = OUT \ PC2$$

3.5.2. ODOMETER AND ALTIMETER SYNCHRONIZING

3.5.2.1. ODOMETER

$$OP1S = POD \ OP2^* \ DT23$$
$$OP1R = OP2 \ WC1^* \ DT23$$

$$OP2S = OP1 \ WC2P \ DT1$$
$$OP2R = WC1^* \ WC2P^* \ DT24$$

$$ON1S = NOD \ ON2^* \ DT23$$
$$ON1R = ON2 \ WC1^* \ DT23$$

$$ON2S = ON1 \ WC2P \ DT1$$
$$ON2R = OP2R$$

$$OC = OP2 \ WC1 \ DT5$$

$$OB = ON2 \ WC1 \ DT5$$

3.5.2.2. ALTIMETER

$$LP1S = PAL \ LP2^* \ DT23$$
$$LP1R = LP2 \ WC1 \ DT23$$

$$LP2S = LP1 \ WC2 \ DT1$$
$$LP2R = WC1 \ WC2^* \ DT24$$

$$LN1S = NAL \ LN2^* \ DT23$$
$$LN1R = LN2 \ WC1 \ DT23$$

$$LN2S = LN1 \ WC2 \ DT1$$
$$LN2R = LP2R$$

$$LC = LP2 \ WC1^* \ DT24$$

$$LB = LN2 \ WC1^* \ DT24$$

3.5.3. STAR SCANNER

3.5.3.1. SCAN MODE CONTROL

GPMS = SC4 PC6 DSO CP5
GPMR = (SSP + MOF + DOF)CP5

ISSS = SC4 PC4 DSO DT2
ISSR = (SSP + MOF + DOF) DT16

SSPS = [SK1* SK2 + NSZ WC1(GPM + SEM)] DT16
SSPR = (ONS + DOF)DT16

3.5.3.2. POLARITY CONTROL

SACS = SC4 PZ DSO CP5
SACR = CSR CP5

SAFS = SC4 PC1 DSO CP5
SAFR = CSR CP5

SECS = SC4 PC2 DSO CP5
SECR = CSR CP5

SEFS = SC4 PC3 DSO CP5
SEFR = CSR CP5

CSR = SC4 PC5 DSO

3.5.3.3. ENABLE

EACS = SC3 PZ DSO CP5
EACR = (SSP + MOF + DOF)CP5

EAFS = SC3 PC1 DSO CP5
EAFR = EACR

EECS = SC3 PC2 DSO CP5
EECR = EACR

EEFS = SC3 PC3 DSO CP5
EEFR = EACR

3.5.3.4. NS REGISTER ZERO DETECTOR

NSZS = DT1
NSZR = NS12P

3.5.3.5. SCAN CONTROL COUNTER

$$3K1S = 3K2^* \; 3W3 \; 3T1 \; DT12$$
$$3K1R = 3K2 \; 337 \; 3T1 \; DT9 + ISS^*$$

$$3K2S = 3K1 \; 3DP^* \; 3T1 \; DT5$$
$$3K2R = 3K1^* \; DT24$$

3.5.3.6. STAR PULSE WIDTH COUNTER

$$3W4PS = 3HS \; ISW^* \; CP5 \qquad\qquad 3W4S = 3W4P \; CP^*$$
$$3W4PR = (3HS^* + ISW)CP5 \qquad\qquad 3W4R = 3W4P^* \; CP^*$$

$$3WnPS = 3Wn{+}1 \; CP5 \qquad n = 3,2,1 \qquad 3WnS = 3WnP \; CP^*$$
$$3WnPR = 3Wn{+}1^* \; CP5 \qquad\qquad 3WnR = 3WnP^* \; CP^*$$

$$3HS = 3W1 \oplus 3HC$$

$$3HCPS = 3DP \; 3T1 \; DT8 \; CP5 \qquad\qquad 3HCS = 3HCP \; CP^*$$
$$3HCPR = 3W1^* \; 3HC \; CP5 \qquad\qquad 3HCR = 3HCP^* \; CP^*$$

$$ISW = IWP \; PC5$$

$$ISWCS = 3W1 \; CP4$$
$$ISWCR = 3W1^* \; CP4$$

3.5.3.7. COARSE PULSE CONTROL

$$3J1S = N36 \; DT2 \; CP5$$
$$3J1R = N36^* \; DT2 \; CP5$$

$$3J2S = \left[3J1^* \; N311 \; 3AF^* \; 3EF^* + 3J1 \; N311^*(3AF + 3EF)\right] ISS \; WC1 \; IN3^* \; DT9 \; CP5$$
$$3J2R = DT8 \; CP5$$

3.5.3.8. SCAN PAST COUNTER

$$3P4PS = (3P1 \oplus 3P4^*)3PGC \qquad\qquad 3P4S = 3P4P \; DT6$$
$$3P4PR = (3P1 \oplus 3P4)3PGC + ISS^* \qquad 3P4R = 3P4P^* \; DT6$$

$$3PnPS = 3Pn \; 3PGC \qquad\qquad 3PnS = 3PnP \; DT6$$
$$3PnPR = 3Pn^* \; 3PGC \qquad\qquad 3PnR = 3PnP^* \; DT6$$

$$3PGC = (3T1 \; 3K2 + 337^* \; 3K2^*)DT6$$

$$SS7 = SP1 \; SP2 \; SP3$$

3.5.3.9. OUTPUT PULSE SYNCHRONIZING

$$ST1S = ST2^* \ FOG \ WC1^*(GPM + ISS)DT3 \ CP5$$
$$ST1R = DT2 \ CP5$$

$$ST2S = ST1 \ DT24 \ CP5$$
$$ST2R = FOG^* \ CP5$$

3.5.3.10. OUTPUT PULSE GATES

$$FAP = SAF^* \ EAF \ ST1$$
$$FAN = SAF \ EAF \ ST1$$
$$CAP = SAC^*(EAC + SJ2 \ ISS)(ST1 + SJ2)$$
$$CAN = SAC(EAC + SJ2 \ ISS)(ST1 + SJ2)$$
$$FEP = SEF^* \ EEF \ ST1$$
$$FEN = SEF \ EEF \ ST1$$
$$CEP = SEC^*(EEC + SJ2 \ ISS)(ST1 + SJ2)$$
$$CEN = SEC(EEC + SJ2 \ ISS)(ST1 + SJ2)$$

3.5.3.11. CARRY AND BORROW

$$SC = (SAF^* \ EAF + SEF^* \ EEF)ISS \ ST1 \ SSP^* \ DT24$$
$$SB = [GPM + ISS (SAF \ EAF + SEF \ EEF)] ST1 \ SSP^* \ DT24$$

3.5.4. EXTRAPOLATOR

$$SEMS = SC2 \ PC4 \ DS0 \ CP5$$
$$SEMR = (MOF + DOF)CP5$$

$$EXOS = SEM \ SSP$$
$$EXOR = MOF + DOF$$

$$EB = SEM \ EXO^* \ WC1^* \ DT24$$

$$SCO = EXO$$

3.6. GYRO TORQUER AND AUTOPILOT

3.6.1. GYRO TORQUER AND AUTOPILOT REGISTER

$$TA21PS = ARS \ OTA + HB3 \ OTA^*$$
$$TA21PR = TA21S^*$$

$$TA21S = TA21P \ CP^*$$
$$TA21R = TA21P^* \ CP^*$$

$$TAnPS = TAn+1 \qquad n = 20,19,.....,1$$
$$TAnPR = TAn+1^*$$

$$TAnS = TAnP \ CP^*$$
$$TAnR = TAnP^* \ CP^*$$

$$TAGC = (WC1^* \ FLT^* + OTA)(DT1-7 + DT9-15 + DT1723)CP5$$

$$OTA = OUT \ PC4$$

3.6.2. GYRO TORQUING PULSE CONTROL

3.6.2.1. POLARITY CONTROL

$$TSXS = TA21 \ OTA \ DT8 \ CP5$$
$$TSXR = TA21^* \ OTA \ DT8 \ CP5$$

$$TSYS = TA21 \ OTA \ DT16 \ CP5$$
$$TSYR = TA21^* \ OTA \ DT16 \ CP5$$

$$TSZS = TA21 \ OTA \ DT24 \ CP5$$
$$TSZR = TA21^* \ OTA \ DT24 \ CP5$$

3.6.2.2. INHIBIT

$$TNXS = [(TSX \ HBK2^* \ TA1^* \ DT7 + TSX^* \ HBK2 \ DT8)TK2 \ TK3^* + FLT]CP5$$
$$TNXR = (OTA \ FLT^* + MOF)CP5$$

$$TNYS = [(TSY \ HBK1^* \ TA1^* \ DT15 + TSY^* \ HBK1 \ DT16)TK2 \ TK3^* + FLT]CP5$$
$$TNYR = TNXR$$

$$TNZS = [(TSZ \ HBK2^* \ TA1^* \ DT23 + TSZ^* \ HBK2 \ DT24)TK2 \ TK3^* + FLT]CP5$$
$$TNZR = TNXR$$

3.6.2.3. OPERATION AND OUTPUT CONTROL

$$TK1S = FOG \ TK3^* \ WC1 \ DT23 \ CP5$$
$$TK1R = DT2 \ CP5$$

$$TK2S = TK1 \ OTA^* \ DT1 \ CP^*$$
$$TK2R = TK3 \ DT23 \ CP5$$

$$TK3S = TK2 \ DT24 \ CP5$$
$$TK3R = FOG^* \ CP5$$

3.6.2.4. OUTPUT PULSE GATES

$$TXP = TSX^* \ TNX^* \ TPG$$
$$TXN = TSX \ TNX^* \ TPG$$

$$TYP = TSY^* \ TNY^* \ TPG$$
$$TYN = TSY \ TNY^* \ TPG$$

$$TZP = TSZ^* \ TNZ^* \ TPG$$
$$TZN = TSZ \ TNZ^* \ TPG$$

$$TPG = TK2 \ TK3 \ OTA^*$$

3.6.2.5. CARRY AND BORROW

$$TC1 = TSY \ TNY^* \ TK2 \ TK3^* \ DT8$$
$$TB1 = TSY^* \ TNY^* \ TK2 \ TK3^* \ DT8$$

$$TC2 = TSX \ TNX^* \ TK1 \ DT24 + TSZ \ TNZ^* \ TK2 \ TK3^* \ DT16$$
$$TB2 = TSX^* \ TNX^* \ TK1 \ DT24 + TSZ^* \ TNZ^* \ TK2 \ TK3^* \ DT16$$

3.7. HALF ADDER B

$$HBS = HBI \oplus HBK$$

$$HBI = (NB1 \ DT1-12 + GA8 \ DT1-12^*)WC1 + TA1 \ WC1^*$$

$$HBK = (NAV^* + DT1-5)HBK1 + NAV \ DT1-5^* \ HBK2 \ WC1 \ DT1-12$$
$$+ HBK1 \ WC1 \ DT1-12^*$$
$$+ (HBK1 \ DT9-16 + HBK2 \ DT9-16^*)WC1^* \ FLT^*$$

$$HBK1PS = (SC + SB + LC + LB + GAC + TC1 + TB1 + EB)CP5 \qquad HBK1S = HBK1P \ CP^*$$
$$HBK1PR = [HBK1(HBC1 \ HBI^* + HBB1 \ HBI) + HBC1^* \ HBB1^*]CP5 \qquad HBK1R = HBK1PR \ CP^*$$

$$HBK2PS = (OC + OB + TC2 + TB2)CP5 \qquad HBK2S = HBK2P \ CP^*$$
$$HBK2PR = [HBK2(HBC2 \ HBI^* + HBB2 \ HBI) + HBC2^* \ HBB2^*]CP5 \qquad HBK2R = HBK2P^* \ CP^*$$

$$HBC1S = (SC + LC + GAC + TC1)CP1$$
$$HBC1R = (DT17 + DT23)CP1$$

$$HBB1S = (SB + LB + TB1 + EB)CP1$$
$$HBB1R = DT17 \ CP1$$

$$HBC2S = (OC + TC2)CP1$$
$$HBC2R = [(DT1 + DT17)WC1 + DT9 \ WC1^*]CP1$$

$$HBB2S = (OB + TB2)CP1$$
$$HBB2R = HBC2R$$

3.8. SERIAL INPUTS TO A REGISTER

$$IO = IADO(IUV + IWD) + IGAO\ IGA$$
$$+ INSO\ INS + IMO\ PC5 + ISWO\ ISW$$

$$IE = IADE(IUV + IWD) + IGAE\ IGA$$
$$+ INSE\ INS + IME\ PC5 + SW1\ ISW$$

3.9. DISCRETE OUTPUTS

ACPS = SZ PZ DSO CP5
ACPR = (SC1 PZ DSO + MOF)CP5

AMIS = SZ PC1 DSO CP5
AMIR = (SC1 PC1 DSO + MOF)CP5

DATS = SZ PC2 DSO CP5
DATR = (SC1 PC2 DSO + MOF)CP5

DIMS = SZ PC3 DSO CP5
DIMR = (SC1 PC3 DSO + MOF)CP5

NCPS = SZ PC4 DSO CP5
NCPR = (SC1 PC4 DSO + MOF)CP5

REDS = SZ PC5 DSO CP5
REDR = (SC1 PC5 DSO + MOF)CP5

SDIS = SZ PC6 DSO CP5
SDIR = (SC1 PC6 DSO + MOF)CP5

FLXS = SZ PC7 DSO CP5
FLXR = (SC1 PC7 DSO + MOF)CP5

MRD = SC3 PC5 DSO

ARMS = SC2 PZ DSO CP5
ARMR = (MOF + DOF)CP5

FCR = SC2 PC1 DSO

FLTS = SC2 PC2 DSO CP5
FLTR = (MOF + DOF)CP5

GANS = SC2 PC3 DSO CP5
GANR = (MOF + DOF)CP5

STAS = SC2 PC4 DSO CP5
STAR = (MOF + DOF)CP5

3.9. DISCRETE OUTPUTS (CONT'D)

MAC   =   SC2 PC6 DS0

TAC   =   SC2 PC7 DSO

HALT   =   SC3 PC4 DSO   COPS   =   COPP COPGC*

                                     COPP   =   COPP* COPGC*

COPPS =   COP* COPGC

COPPR =   COP COPGC

COPGC =   SC3 PC7 DSO DT9

DOF   =   SC4 PC7 DSO

GLOSSARY OF LOGICAL TERMS

Term	*	Section	Description
AB	S	2.1	**A Register Even Bit Delay.** Used in DIV operation for obtaining one bit left shifted sum (from A Register) as Augend (X) input to Adder. Used in MPY operation to remember sign of A Register at last bit time (LBT).
ABGC	L	1.9	**ABR Gated Clock.** Provides either 1 mc. or 500 KC clock pulses for shifting the ABR.
ABR		1.9	**Memory Address Buffer Register** (AB1-AB12)
AB1 ' ' ' ' ' AB12	S S	1.9 1.9	**Memory Address Buffer Register.** A 12 bit serial register which accepts the address of the memory location to be accessed during the next word time. In normal operation, (no transfer or interrupt) operand addresses are shifted in during C2 (from IC) and C0 (from S4) and the next instruction address is shifted in during C1 (from S3). The ABR is initialized from the Instruction Counter entry keys on the MCU when En=1.
AC	S	1.8	**Absolute Address Control.** Set at beginning of DT10 if next instruction to be executed refers to working storage $(7600 - 7777)_8$ for its operand.
ACP	S	3.9	**Accepted Check Point Discrete Output Flip-Flop.** Set code 7300. Reset code 7320.
AD	L	2.6	**Add/Subtract Control.** Used in CY1 and CY2 logic to cause S1 and S2 to produce either a sum or difference.
ADD	L	1.3	**Add Command.** Decoded from Operation Code Register (OR1-OR6). Used in A Register and AU Adder Logic to control the addition (2 bits at a time at 250 kc) of the contents of the selected memory location to the contents of the A Register, with the sum replacing the initial contents of the A Register.
AGC	L	2.1	**A Register Gated Clock.** Allows the A Register to be shifted only when used. The A Register shifts at 1 mc (2 bits at a time) during execution phase of MPY, DIV, LRS and RTE, and shifts at 250 kc (2 bits at a time) at all other times when used.
AMI	S	3.9	**Accepted Manual Input Discrete Output Flip-Flop.** Set code 7302. Reset code 7322.
APU		3.0	**Accelerometer Processing Unit**
AR		2.1	**A Register** (A1-A24)

*S = Storage Element Output   L = Logical Gate Output
 T = Timing Signal   I = Computer Input Signal

ARM	S	3.9	**Arm Warhead Discrete Output Flip-Flop.** Set code 7340. Reset code 7317 (DOF). Also reset by MOF.
ARS	L	2.1	**A Register Serial Output.** Converts A Register output from 2 bits parallel - serial at 250 kc to one bit serial at 500 kc for purpose of communication with Input/output Registers and MCU.
ASM	S	3.1.2	**Accelerometer Registers Sign Storage Flip-Flop.** Copies and holds sign bits of Accelerometer pulse accumulations so that the signs will be extended into bit positions 10 through 12 and 22 through 24 when the information is read into the A Register.
AU		2.0	**Arithmetic unit**

Table 1

	R	Q	
	0	0	
	0	1	
	1	1	
	1	0	
	0	0	

Table 2

t		t – 1			
R1	Q1	R2	Q2	C	B
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	–	–
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	–	–
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	–	–
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	–	–
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	0
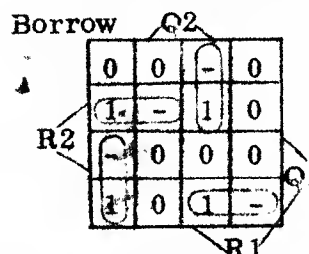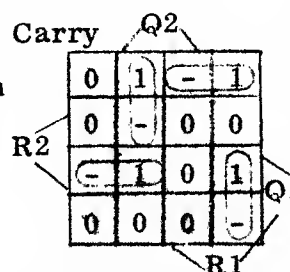
| AUB | S | 3.1.1 | U Axis Accelerometer Borrow Storage Flip-flop. Set at beginning of DT24 if a unity subtract (borrow) condition is detected by the synchronizing flip-flop (AUR1, AUR2, AUQ1, AUQ2). Carry (C) or Borrow (B) is detected in accordance with the truth table as shown in Table 2. Input signals R (Reference) and Q (Quadrature) present a Gray Code sequence as shown in Table 1, with a change in the direction of the negative arrow required to produce a Borrow (B) and a change in the positive direction required to produce a Carry (C). |

Carry map (R2, R1 rows; Q2, Q1 columns):

	Q2			
	0	1	–	1
R2	0	–	0	0
	–	1	0	1
	0	0	0	–
				Q1 / R1

Borrow map:

	Q2			
	0	0	–	0
R2	1	–	1	0
	–	0	0	0
	1	0	1	–
				Q1 / R1

The R and Q signals are synchronized by the R1 and Q1 flip-flops which are copied, in turn, by the R2 and Q2 flip-flops. Therefore, if R1 and Q1 represent the states of the inputs at time t, R2 and Q2 represent the previous states or the states at time t–1.

AUC	S	3.1.1	U Axis Accelerometer Carry Storage Flip-flop. Set at beginning of DT24 if a unity Add (Carry) condition is detected. See above discussion.
AUQ1	S	3.1.1	U Axis Accelerometer Quadrature Signal Synchronizing Flip-flop. Copies Quadrature Signal at end of DT23.
AUQ2	S	3.1.1	U Axis Accelerometer Quadrature Signal Synchronizing Delay Flip-flop. Copies AUQ1 at end of DT24.
AUR1	S	3.1.1	U Axis Accelerometer Reference Signal Synchronizing Flip-flop. Copies Reference Signal at end of DT23.
AUR2	S	3.1.1	U Axis Accelerometer Reference Signal Synchronizing Delay Flip-Flop. Copies AUR1 at end of DT24.
AVB AVC AVQ1 AVQ2 AVR1 AVR2	S	3.1.1	See description for AUB through AUR2. Substitute V for U, DT5 and DT6 for DT23 and DT24 respectively. Timing is shifted so that a common unity Add/Subtract unit can be used for all 3 accelerometers and real time.

AWB AWC AWQ1 AWQ2 AWR1 AWR2	S	3.1.1	See description for AUB through AUR2. Substitute W for U and DT11 and DT12 for DT23 and DT24 respectively. Timing is shifted so that a common unity Add/Subtract unit can be used.
A1 ? ? ? ? A24	S	2.1	Accumulator Register. A 24 bit register used in all Arithmetic and Input/Output operations except DSO. May be considered as two 12 bit shift registers with a common gated clock, one register holding the even numbered bits and the other register holding the odd numbered bits. See description of individual commands (ADD, SUB, MPY, etc.) for further details
BB	S	2.2	B Register Even Bit Delay Flip-flop. Used in the execution of the DIV command to allow the least significant half of the double length dividend to be left shifted one bit position during each 12 μs cycle.
BC	S	1.3	IBR to OCR Transfer Control. Provides a 2 μs pulse when the IBR is to be parallel transferred to the OCR.
BGC	L	2.2	B Register Gated Clock. Allows the B Register to be shifted only when used. The B Register shifts at 1 mc (2 bits at a time) during the execution phase of MPY, DIV, LRS and RTE, and shifts at 250 kc (2 bits at a time) at all other times when used.
BIE	S	1.7	Bias Register and Instruction Counter Even Bit Flip-Flop. Used to store the even bits of the Instruction Counter (during DT1-12) and Bias Register (during DT13-24) in preparation for transfer to the even half of the M Register during the first word (PC7) of execution of the TRS command.
BIO	S	1.7	Bias Register and Instruction Counter Odd Bit Flip-Flop. Same function as BIE for odd bits.
BIS	S	1.8	Bias Register or Instruction Counter Select Flip-Flop. Used in the Memory Address Adder Logic to select the source of the Addend Input (Y4) for the computation of the effective address of the Operand to be used in the next command to be executed. BIS is set at the beginning of DT10 if the next command is a JOM or uses an Instruction Counter Referenced Operand. Otherwise it is reset.

BR		2.2	B Register (B1 - B24)

BRGC | L | 1.7 | <u>Bias Register Gated Clock</u>. Allows the Bias Register to be shifted at either 1 mc or 500 kc depending on the command being executed. The Bias Register shifts at 1 mc during DT12 through DT17 at all times except during the first word of TRA and TRS, when it shifts at 500 kc during DT13 through DT24. It also shifts at 500 kc during DT18 through DT23 of SBR.

BR1 | S | 1.7 | <u>Bias Register</u>. A 12 bit shift register used as an alternative reference for relative addressing of operands. The contents of the Bias Register may be changed indirectly by a TRA or TRS command or directly by an SBR or MBR command. At all other times the contents remain unchanged.

BR12 | | | See description of TRA, TRS, SBR and MBR for further details

BSR | | | Bias Register (BR1 - BR12)

B1 | S | 2.2 | <u>Multiplier - Quotient (B) Register</u>. A 24 bit register used in execution of MPY, DIV, LRS, RTE and XAB. May be considered as two 12 bit shift registers with a common gated clock, one register holding the even numbered bits and the other register holding the odd numbered

B24 | | | bits. See description of above commands for further details.

CAGC | L | 1.4 | <u>Control Counter and Input/Output Address Register Gated Clock.</u> Provides a clock at the end of each C0 and C1 word for transfer of address field into CA1 through CA6 or for decrementing during the long commands. Also provides a 1 mc clock for LRS and RTE.

CAN | L | 3.5.3 | <u>Coarse Azimuth Negative and Positive Pulses</u>. The output signals to the Star Scanner Coarse Azimuth digital servo. Pulses are generated under program control at a 7.5 ms interval in the Gross Positioning Mode (GPM = 1) and at a 960 ms interval in the Star Scanning Mode (ISS = 1).

CA1 | S | 1.4 | <u>Control Counter and Input/Output Address Register</u>. A 6 bit register used as a word counter for long commands (MPY, DIV, TRA and TRS), as a shift counter for LRS and RTE and as an address register for INP, OUT, DSI and DSO. In MPY, DIV, TRA and TRS the 3 least significant bits (CA1, CA2, CA3) are set prior to command execution and decremented binarily at the end of each word time until CZ = 1. In all other commands the address field (IB13 through IB18) of the instruction is parallel transferred into the Control Counter as shown, prior to command execution.

Symbol			
	S	1.4	Instruction Buffer Register

Instruction Buffer Register

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | — — — | 1 |

| 6 | 5 | 4 | 3 | 2 | 1 |

Control Counter

Symbol	Type	Ref	Description
CA6			In LRS and RTE the Control Counter is decremented at a 1 mc rate until CA1 through CA5 are all zero.
CC	S	1.8	**Complement Control Flip-flop.** For relative addressing CC is used to extend the sign bit (initially in IB18) of the instruction address field for the effective address computation. For absolute addressing it is used to force "1"s into the four most significant bits of the 12 bit memory address.
CEN	L	3.5.3	**Coarse Elevation Negative and Positive Pulses.** The output signals to the
CEP	L	3.5.3	Star Scanner Coarse Elevation digital servo. Pulse rates same as CAN, CAP.
CME	L	1.1	**Core Memory Even Bit Gate.** Presents the even bits to be written into memory. Except for STO and the last word of TRS these are the bits just read. In STO they are the even bits of the A Register and in the last word of TRS they are the even bits at the M Register (which contains the old Instruction Counter and Bias Register contents to be stored in memory location zero).
CMO	L	1.1	**Core Memory Odd Bit Gate.** Same function as CME for odd bits.
CMS	L	1.1	**Core Memory Serial Gate.** Combines CME and CMO to produce a 500 kc serial signal for input to the Instruction Buffer Register, Instruction Counter and Bias Register.
CP*	T		**1 mc Clock** occurring between CP1 pulses.
CPS	T		**Strobe Clock.**
CP1	T		**1 mc Clock.**
CP3	T		**250 kc Clock.** Coincident with CP5 during EDT.
CP4	T		**250 kc Clock.** Coincident with CP5 during ODT.
CP5	T		**500 kc Clock.** Coincident with 2nd CP1 in all digit times.
CP6	T		**500 kc Clock.** Coincident with 1st CP1 in all digit times.
CP7	T		**250 kc Clock.** Coincident with CP6 during ODT.
CP8	T		**250 kc Clock.** Coincident with CP6 during EDT.

CSR	L	3. 5. 3	<u>Common Sign Reset.</u> A one word time discrete output signal used to reset the 4 Star Scanner Polarity Control Flip-Flop. Code 7313.
CY1	S	2. 6	<u>Odd Bit Address Carry Flip-Flop.</u> Provides carry/borrow storage for the carry or borrow into the Odd Bit Adder.
CY2	L	2. 6	<u>Even Bit Adder Carry Gate.</u> Provides the carry/borrow function for the carry or borrow into the Even Bit Adder.
CY3	S	1. 6	<u>Instruction Count Incrementer Carry Flip-Flop.</u> Provides carry storage for incrementing the instruction count.
CY4	S	1. 8	<u>Operand Address Adder Carry Flip-Flop.</u> Provides carry storage for the effective address computation.
CZ	L	1. 3	<u>Control Zero.</u> Designates the last word time of the long commands (MPY, DIV, TRA, TRS).
CO	L	1. 5	<u>Zero State of Operation Cycle Counter.</u> Normally true for one word time (48 µs) unless a long instruction (MPY, DIV, TRA, TRS) is being executed.
C1	S	1. 5	<u>Operation Cycle Counter.</u> A two stage, three state counter used to control the operation sequence of the Instruction Processing Unit. For
C2	S	1. 5	normal operation (no Interrupt or Transfer) the sequence is as follows:

State	C2	C1	Serial Information Flow
C2	1	0	Read in two 12 bit instructions from memory location n into Instruction Buffer Register (IBR).
C0	0	0	Execute right hand instruction from memory location n-1. Compute effective address of operand for left hand instruction from location n and place in Memory Address Buffer Register (ABR).
C1	0	1	Execute left hand instruction from memory location n. Compute effective address of operand for right hand instruction from location n and place in Instruction Counter (IC), while simultaneously placing the incremented contents of IC, (n + 1), in ABR.
C2	1	0	Read in two 12 bit instructions from memory location n + 1 into IBR. Place contents of IC (effective address of right hand n operand) in ABR, while simultaneously placing the contents of ABR, (n + 1), in IC.
C0	0	0	Execute right hand n instruction, etc.
C1	0	1	

DAT	S	3.9	<u>Output to Data Link Discrete Output Flip-flop.</u> Set code 7304. Reset code 7324. Also reset by MOF.
DC	S	2.5	<u>Divide Control Flip-flop.</u> See DIV.
DEC	L	1.4	<u>Decrement Control Counter Signal.</u> Enables binary countdown logic for CA1 through CA5.
DIM	S	3.9	<u>Brightness Gain Change Discrete Output Flip-flop.</u> Set Code 7306. Reset Code 7326. Also reset by MOF.
DIV	L	1.3	<u>Divide Command.</u> Decoded from Operation Code Register. Used to control gating in AU and IPU for execution of Divide command. During DIV the Operation Cycle Counter remains locked in either C0 or C1 and the Control Counter counts down to zero (PZ = 1) from its initial setting of 7 (PC7 = 1) at the word time rate. The dividend is assumed to be in the combined A (most significant half) and B (least significant half) Registers at the beginning of PC7. The divisor is shifted into the M Register from memory during PC7. At the end of PC7 the sign bits of the divisor and the dividend are compared and the Divide Control Flip-flop (DC) is set or reset depending on whether the signs are the same or different. During DT1 through DT6 of PC6 the divisor is subtracted from or added to the 1 bit left shifted dividend depending on whether DC is true or false. Subsequent changes in DC are made on the basis of comparison of A1 and CY2 at last bit time (LBT) which occurs every 12 μs (6 digit times). DC has the dual function of controlling the Add/Subtract decision and holding the quotient bits which are entered into the least significant end of the B Register as the least significant bits of the dividend are shifted out. At the end of 24 Add/ Subtract cycles (6 word times) the quotient (with sign bit inverted) is in the B Register and the residue is in the A Register. During PZ the A and B registers are exchanged and the quotient sign bit corrected.
DOF	L	3.9	<u>Discrete Outputs Off Signal.</u> Used to reset certain discrete output flip-flops. Code 7317.
DRR	I	2.8	<u>Data Register Ready Discrete Input Signal.</u> Code 7256.
DSI	L	1.3	<u>Discrete Input Command.</u> Decoded from Operation Code Register. Used in conjunction with Input/Output Address Register (CA1 - CA6) decoding to cause sign bit of A Register (A24) to be set or reset depending on whether the selected Discrete Input is true or false. A1 through A23 are unaffected.

| DSO | L | 1. 3 | **Discrete Output Command.** Decoded from Operation Code Register. Used in conjunction with Input/Output Address Register (CA1-CA6) decoding to control Discrete Output flip-flops and signals, the Extrapolator Mode flip-flop and the Star Scanner Polarity and Enable flip-flops. |

DT1	T		**Digit Time 1**
↓	↓		
DT24	T		**Digit Time 24** — Sequential timing pulses of 2 μs duration each occurring every 48 μs.

| DTm-n or DTmn | T | | **Digit Times m through n inclusive.** |

| DY | L | 1. 3 | **Long Command Signal.** True during MPY, DIV, TRA, TRS. |

D1 S 2. 4
D2 S
D3 S

Multiply Control Register. A 3 stage register used to control the addition or subtraction of the multiplicand (in the M Register) to or from the partial product (in the A Register). The D1-D3 input logic performs the indicated transformation from the least significant multiplier bits at the end of each add cycle to control the operation during the following cycle. (Note that the B Register precesses two bits to the right with respect to the 13 us add cycle). D1 and D2 are used to control whether the multiplicand or twice the multiplicand is used as the addend (Y1 and Y2) input. D3 determines whether an addition or subtraction is performed.

B4	B3	B2	A	D3	D2	D1
0	0	0	0	0	0	0
0	0	1	+1	0	0	1
0	1	0	+1	0	0	1
0	1	1	+2	0	1	0
1	0	0	-2	1	1	0
1	0	1	-1	1	0	1
1	1	0	-1	1	0	1
1	1	1	0	1	0	0

EAC	S	3.5.3	**Enable Azimuth Coarse Flip-flop.** Set code 7360. Reset by Scanner Servo Positioned (SSP) flip-flop, DOF or MOF. Used to control Coarse Azimuth Pulse gates (CAN and CAP) during GPM.
EAF	S	3.5.3	**Enable Azimuth Fine flip-flop.** Set code 7362. Reset same as EAC. Used to control Fine Azimuth Pulse gates (FAN and FAP) during GPM and ISS.
EB	L	3.5.4	**Extrapolator Borrow Signal.** A 2 µs pulse occurring every 96 µs in the Extrapolator Mode (SEM = 1) when the NS Register is non-zero. Causes the NS Register to decrement every other word time until it reaches zero.
EDT	T		**Even Digit Time.** A 250 kc square wave, true in all even numbered digit times.
EEC	S	3.5.3	**Enable Elevation Coarse Flip-flop.** Set code 7364. Reset same as EAC. Used to control Coarse Elevation Pulse gates (CEN and CEP) during GPM.
EEF	S	3.5.3	**Enable Elevation Fine Flip-flop.** Set code 7366. Reset same as EAC. Used to control Fine Elevation Pulse gates (FEN and FEP) during GPM and ISS.

EN	S	1.13	ENTCTR Synchronizing Flip-Flop. Synchronizes the ENTCTR signal from the MCU with the computer word time. Used in AB Register logic to allow new Instruction Counter setting to be read in from the MCU during computer idle mode (IDL).
ENTCTR	I	1.13	Enter Instruction Counter - signal from MCU.
ENTKYS	I	1.2 1.9	Serial Information Line from MCU Control Register. When EN is true it presents the address which had been set in the Instruction Counter octal switches. When EX is true it presents the two instructions which had been set in the Instruction Entry switches.
EX	S	1.13	EXINST Synchronizing Flip-flop. Synchronizes the EXINST signal from the MCU with the computer word time. Used in IB Register logic to allow instructions to be read in from the MCU.
EXINST	I	1.13	Execute Instruction - signal from MCU.
EXO	S	3.5.4	Extrapolator Zero Flip-flop. Set during word time that NS Register reaches zero in Extrapolator Mode. Reset by MOF or DOF.
FAN FAP	L L	3.5.3 3.5.3	Fine Azimuth Negative and Positive Pulses. The output signals to the Star Scanner Fine Azimuth digital servo. Pulses are generated under program control at a 7.5 ms interval in both the Gross Positioning Mode (GPM = 1) and the Star Scanning Mode (ISS = 1).
FBT	L	2.7	First Bit Time. A one microsecond pulse occurring every 13 μs during MPY and every 12 μs during all other operations. Decoded from Multiply-Divide Bit Counter (MC1-MC4). Used in DIV to designate time to place quotient bit (from DC) in B23 of B Register.
FCGC	L	3.3.1	400 Cycle Counter Gated Clock. Presents a synchronized pulse when the 400 cycle reference signal (GF) goes negative. Used to clock the 400 Cycle Counter.
FCR	L	3.9.1	Flexowriter Carriage Return Discrete Output. Code 7342.

FC1	S	3.3.1	400 Cycle Counter. A four stage, twelve state shift logic type
FC2	S	3.3.1	counter. Used in the generation of 1) the Interrupt signal (INT),
FC3	S	3.3.1	2) the Gyro Torquing Pulses (TXN, TXP, TYN, TYP, TZN, TZP),
FC4	S	3.3.1	3) the Star Scanner Servo Pulses (CAN, CAP, CEN, CEP, FAN,
			FAP, FEN, FEP) and 4) the Gimbal Angle Counter Control
			(GC1 - GC4).

4	3	2	1	←GC	Operation
1	0	0	0	1	Output Servo Pulse (FOG = 1)
0	1	0	0	2	
1	0	1	0	3	
0	1	0	1	4	Reset GA Register (FRG=1), Output Servo Pulse (FOG=1)
0	0	1	0	5	Count Alpha Gimbal Angle
1	0	0	1	6	Generate INT (middle of interval)
1	1	0	0	7	Count Gamma Gimbal Angle, Output Servo Pulse (FOG=1)
1	1	1	0	8	Count Beta Gimbal Angle
0	1	1	1	9	
0	0	1	1	10	Reset GA Register (FRG=1), Output Servo Pulse (FOG=1)
0	0	0	1	11	
0	0	0	0	12	
1	0	0	0	1	Output Servo Pulse (FOG=1)

FEN	L	3.5.3	Fine Elevation Negative and Positive Pulses. The output signals to the
FEP	L	3.5.3	Star Scanner Fine Elevation Digital Servo. Pulse rates same as FAN,
			FAP.

| FLT | S | 3.9 | Flight Mode Discrete Output Flip-flop. Set code 7344. Reset by MOF |
| | | | or DOF. |

| FLX | S | 3.9 | Flexowriter On Discrete Output Flip-flop. Set code 7316. Reset code |
| | | | 7336. Also reset by MOF. |

| FLY | I | 2.8 | Initiate Airborne Computations Discrete Input. Code 7206. |

FOG	L	3.3	133 Cycle Output Pulse. Derived from 400 Cycle Counter (FC1-FC4).
FRG	L	3.3	Gimbal Angle Counter Reset Signal. Derived from 400 Cycle Counter (FC1-FC4).
GA	I	3.3	Alpha Gimbal Angle Input. A 400 cycle square wave with phase displacement from GF equal to Gimbal Angle Alpha.
GAC	L	3.4.2	Gimbal Angle Carry. Produces a synchronized signal to increment the high order counter (GA8 - GA12) with each overflow of GA7. The carry is synchronized to occur during the alternate word time when the high order counter is using the Unity Add/Subtract Unit (HBS).
GAE	L	3.4.3	Gimbal Angle Counter Scan Logic - Even Bits. Performs parallel to serial conversion of odd numbered bits of low order counter (GA1-GA7) and gates odd bits of high order counter to IGAE flip-flop. See IGA.
GAGC	L	3.4.3	Gimbal Angle High Order Counter Gated Clock. Provides 500 kc clock pulses when counter is being incremented, recirculated or cleared.
GAN	S	3.9	Autopilot Gain Change Discrete Output Flip-flop. Set code 7346. Reset by MOF or DOF.
GAO	L	3.4.3	Gimbal Angle Counter Scan Logic - Odd Bits. Performs parallel to serial conversion of even numbered bits of low order counter (GA1-GA7) and gates even bits of high order counter to IGAO flip-flop. See IGA.
GA1	S	3.4.2	Gimbal Angle Counter - Low Order. A 7 stage, 1 mc, straight binary counter. The counter is set (to all 1's) by FRG prior to the alpha count interval. During the alpha count interval it counts while GC4=1. During the Interrupt interval the count is read out into the A Register (IGA=1) and the counter is reset. During the first halves of both the gamma and beta count intervals the counter counts while
GA7	S	3.4.2	GC4=1 and is read out and reset during the last halves.
GA8	S	3.4.3	Gimbal Angle Counter - High Order. A 5 stage serial shift register which increments on the overflow of GA7 during the gimbal angle count intervals. The register is set (to all 1's) by FRG and also upon
GA12	S	3.4.3	readout to the A Register (IGA=1).

GB	I	3.4.1	Beta Gimbal Angle Input. A 400 cycle square wave with phase displacement from GF equal to Gimbal Angle Beta.
GC	I	3.4.1	Gamma Gimbal Angle Input. A 400 cycle square wave with phase displacement from GF equal to Gimbal Angle Gamma.
GCG	L	3.4.1	Gimbal Angle Count Gate. A signal which is true during the phase displacement interval of each of the 3 count intervals. The phase displacement interval is defined as the interval from the fall of the reference signal (GF) to the fall of the angle signal (GA, GB or GC). For beta and gamma angles greater than 180°, the phase displacement interval is undefined.
GC1 GC2	S S	3.4.1 3.4.1	GF Trailing Edge Synchronizer. GC1 produces a 400 cycle pulse of $1\mu s$ duration in synchronism with the trailing edge of GF. This pulse is used (in FCGC) to step the 400 Cycle Counter and in the set logic of GC3.
GC3	S	3.4.1	Alpha $> 180^\circ$ Detector. This flip-flop is set at the beginning of the alpha count interval if the alpha gimbal angle is greater than 180°. Used in count gate logic GCG.
GC4	S	3.4.1	GCG Synchronizing Flip-flop. Synchronizes GCG with 1 mc clock.
GC5 GC6	S S	3.4.2 3.4.2	Gimbal Angle Low Order Counter Overflow Detector and Synchronizing Flip-flops. Detects and holds the $1\mu s$ overflow signal (GA7PR) until the high order counter (GA8-GA12) is incremented.
GF	I	3.3 3.4.1	400 Cycle Reference Signal. A 400 cycle square wave used in the 400 Cycle Counter and Gimbal Angle Counter Control Logic.
GPM	S	3.5.3	Gross Positioning Mode Flip-flop. Set code 7315. Reset when Scanner Servo Positioned Flip-flop is set (SSP=1). Also reset by MOF or DOF. Used in Star Scanner logic to enable borrow pulses (SB) to be generated for decrementing the NS Register and to enable the Output Pulse Sync. (ST1). During Gross Positioning Mode the Star Scanner is slewed from the index position to a predetermined star position under program control.
GRG	L	3.4.2	Gimbal Angle Low Order Counter Reset Gate. Used to set GA1-GA8 when FRG is true and also when the GA Register is read into the A Register (IGA=1).

HAI	L	3.1.3	**Half Adder A Serial Input.** Gates UV and WD Registers to Half Adder A (HAS)
HAK	S	3.1.3	**Half Adder A Carry Flip-flop.** Used as a common second rank flip-flop for the 4 primary rank carry flip-flops (HUK, HVK, HWK, HDK).
HALT	L	3.9	**Halt Discrete Output Signal to MCU.** Code 7370.
HAS	L	3.1.3	**Half Adder A Sum Output.** Used to recirculate and increment UV and WD Registers.
HAT	S	3.1.3	**Half Adder A Timing Flip-flop.** Used in control of carry Flip-flops (HUK, HVK, HWK, HDK).
HAW	S	3.1.3	**Alternate Word Flip-flop.** Used to increment real time segment of WD Register at a frequency of 10 kc.
HBB1	S	3.7	**Half Adder B Borrow Storage Flip-flop No. 1.** Detects the 2 μs borrow pulses from the Star Scanner (SB) Altimeter (LB) Gyro Torquer (TB1) and Extrapolator (EB) logic and causes HBK1 to be reset on the first "1" bit from the serial input (HBI) for decrementing.
HBB2	S	3.7	**Half Adder B Borrow Storage Flip-flop No. 2.** Detects the 2 μs borrow pulses from the Odometer (OB) and Gyro Torquer (TB2) logic and causes HBK2 to be reset on the first "1" bit from the serial input (HBI) for decrementing.
HBC1	S	3.7	**Half Adder B Carry Storage Flip-flop No. 1.** Detects the 2 μs carry pulse from the Star Scanner (SC) Altimeter (LC) Gimbal Angle Counter (GAC) and Gyro Torquer (TC1) and causes HBK1 to be on the first "0" bit from the serial input (HBI) for incrementin
HBC2	S	3.7	**Half Adder B Carry Storage Flip-flop No. 2.** Detects the 2 pulses from the Odometer (OC) and Gyro Torquer TC2 and causes HBK2 to be reset on the first "0" bit from the serial input (HBI) for incrementing.

HBI	L	3.7	**Half Adder B Serial Input.** Gates TA, NS and GA Registers to Half Adder B in accordance with following table:

Mode	WCI	DT	Function	Data Location	Carry/Borrow Pulse	Carry-FF
NAV	0	1-7	Gyro - X Axis	TA1-TA7	TC2, TB2	HBK2
NAV	0	9-15	Gyro - Y Axis	TA8-TA14	TC1, TB1	HBK1
NAV	0	17-23	Gyro - Z Axis	TA16-TA21	TC2, TB2	HBK2
NAV	1	1-5	Altimeter	NS1-NS5	LC, LB	HBK1
NAV	1	6-12	Odometer	NS6-NS12	OC, OB	HBK2
NAV	1	18-23	Gimbal Angles	GA8-GA12	GAC	HBK1
FLT	0	1-7	Autopilot - Yaw Axis	TA1-TA7	(None)	–
FLT	0	9-15	Autopilot-Roll Axis	TA8-TA14	(None)	–
FLT	0	17-23	Autopilot-Pitch Axis	TA16-TA21	(None)	–
FLT	1	1-12	Extrap/Scanner	NS1-NS5	EB, SB, SC	HBK1
FLT	1	18-23	Gimbal Angles	NS6-NS12	GAC	HBK1

HBK	L	3.7	**Half Adder B Carry Input.** Gates HBK1 and HBK2 to Half Adder B in accordance with preceding table.
HBK1 HBK2	S	3.7	**Half Adder B Carry/Borrow Flip-flops.** Operate as Carry/borrow flip-flops for incrementing and decrementing functions as indicated in the preceding table.
HBS	L	3.7	**Half Adder B Sum Output.** Used to recirculate and increment TA, NS and GA Registers.
HDK	S	3.1.3	**Real Time Carry Flip-flop.** Used to increment real time counter in WD Register.
HUK HVK HWK	S S S	3.1.3 3.1.3 3.1.3	**Accelerometer Carry/Borrow Flip-flops.** Used to increment or decrement Accelerometer counters in UV and WD Registers.
IAA	L	2.8	**Index Angle Achieved Discrete Input.** Code 7210.
IADE	S	3	**Input Accelerometer and Real Time Registers - Even Bits.** Holds even bits of UV and WD Registers to be read into A Register.

IADO	S	3.1.2	**Input Accelerometer and Real Time Registers – Odd Bits.** Holds odd bits of UV and WD Registers to be read into A Register.
IBGC	L	1.2	**Instruction Buffer Register Gated Clock.** Allows IBR to shift at 500 kc during instruction read in and at 1 mc during effective address computation and half rotation.
IBR		1.2	**Instruction Buffer Register** (IB1 – IB24).
IB1	S	1.2	**Instruction Buffer Register.** A 24 bit shift register used to buffer
IB24	S	1.2	the instructions as they are read in from memory to recirculate the instructions for the purpose of the effective address computation.

OCC	DT	Shift Rate	Operation
C2	1-24	500 kc	CMS→IB24. Read in two 12 bit instructions.
C0	12-23	1 mc	Full recirculation. IB13→X4 to form operand address for next C1 executed instruction.
C1	2-7	1 mc	Half recirculation to place right hand instruction in IB13 – IB24.
	12-23·	1 mc	Full recirculation. IB13→X4 to form operand address for next C0 executed instruction.
C2	1-24	500 kc	Repeat cycle.

IC		1.6	**Instruction Counter** (IC1-IC12)
ICGC	L	1.6	**Instruction Counter Gated Clock.** Allows Instruction Counter to be shifted at either 500 kc or 1 mc depending on operation.
ICP	L	2.8	**Insert Check Point Discrete Input.** Gode 7212
IC1	S	1.6	**Instruction Counter.** A 12 bit **serial register used to buffer 1) the instruction**
IC12	S	1.6	address, and 2) the operand address of the instruction to be executed during C0.

IC1 (con't)	S	1. 6

OCC	DT	Shift Rate	Input	Output
C2	12-17	1 mc	AB1→IC12. Instruction address n	IC1→AB12. Operand address for next C0 executed instruction.
C0	12-17	1 mc	IC1→IC12. (Recirculate)	IC1→Y4 (BIS=1) to form operand address for next C1 executed instruction.
C1	12-17	1 mc	S4→IC12. Operand address for next C0 instruction	IC1→Y4 (BIS=1) to form operand address for next C0 executed instruction.
C2	12-17	1 mc	AB1→IC12. Instruction address n+1. Repeat cycle.	IC1→AB12.

ID	L	2. 8

Discrete Input Selection Gate. Combines Discrete Input signals and Input/Output Address Register states (PC3-PC7 and SZ-SC3).

IDL	S	1. 12

Computer Idle Flip-flop. Set at the beginning of C2 if LOGIDL is true. During IDL all AU and IPU registers are either recirculated for output to the MCU or held static as indicated. Input/Output registers are unaffected.

Register		Data Rate		
AR	Recirculated	250 kc	2 bit parallel
BR	Static		
MR	Static		
IBR	Recirculated	500 kc	Serial
OCR	Static		
CAR	Static		
OCC	Static		
BSR	Recirculated	500 kc	Serial
IC	Recirculated	500 kc	Serial
ABR	Recirculated	500 kc	Serial
MAR	Static		

IE	L	3. 8

Input Even bit. Presents even bits of program selected input registers to the A Register logic.

IGA	L	3.4.3	Input GA Counter to A Register. Selects GA Counters to be read into A Register. Used in GA Counter logic to cause all counter stages to be set following readout. The GA Counter GA1 – GA12 is read into bit positions 12 through 23 of the A Register and the sign bit (A24) is always positive (zero). Therefore the odd numbered bits of GA (GA1, GA3, etc.) are read into even positions of A (A12, A14, etc.) and vice versa.
IME	I	3.8	Input MCU Data Register – Even Bits. Even bit data input line from MCU Data Register.
IMO	I	3.8	Input MCU Data Register – Odd Bits. Odd bit data input line from MCU Data Register.
INP	L	1.3	Input Command. Decoded from Operation Code Register. Used in A Register logic to allow IE and IO to be shifted in.
INS	L	3.5.1	Input NS Register. Selects NS Register to be read into A Register. Used in NS Register logic to cause all register stages to be reset following readout. The NS Register is read into bit positions 13 through 24 of the A Register.
INSE	S	3.5.1	Input NS Register – Even Bits. Holds even bits of NS Register to be read into A Register.
INSO	S	3.5.1	Input NS Register – Odd Bits. Holds odd bits of NS Register to be read into A Register.
INT	L	1.11	Interrupt Signal. A variable length (T > 48 μs) logically generated pulse occurring every 30 ms. In the compute mode (IDL = 0) INT goes true in the middle of the Interrupt state of the 400 Cycle Counter, and initiates the Interrupt sequence. During the Interrupt sequence the following operations occur: 1) Program control is transferred from location n to location 7777 where the instruction pair No Op, TRS(AT) is stored (assuming that the Interrupt subroutine is to be executed). 2) The incremented IC (n+1) and the BSR settings are stored in location 0001. 3) The IC and BSR settings for the Interrupt subroutine are obtained from location AT. 4) The subroutine is executed. The last word of the subroutine contains a TRA (001) instruction which returns program control back to location n+1. For specific dtails of timing and information flow see next page.

Timing diagram with rows: CAR, OCC, DT, INT, INT3, INT1, INT4, INT2, and a lower table of registers:

Instruction Executed		I Ln	(None)	IRn	No op	(None)	
Memory	In	OLn	[7777]	ORn	0 – No op	[n+1]	AS
	Out	OLn	[7777] = No op, TRS (AT)	ORn	0 – No op	[n+1]	AS
IBR	In	R	CMS [7777]	R	R/2	R	CMS [n+1]
	Out	R/2	IRn, ILn				TRS(AT), No op
IC	In	S4 (ARn)	MR (n)	R	S4 (AT)	ABR (n+1)	CMS(AS)
	Out	n	ARn		n	AT	n + 1
BSR	In	R	R	R	R	R	CMS (
	Out						BSa
ABR	In		IC (ARn)	S4 (A-No op)	S3 (n + 1)	IC (AT)	IC
	Out	ALn 7777	7777	ARn	A – No op	n + 1	A
MAR		A Ln	7777	ARn	A – No op	n + 1	AT
MR	In	IC (n)	0			IC(n+1)	BSR(B
	Out		n				

n = Instruction Address n
ALn = Operand Address for left instruction from Location n
ARn = Operand Address for right instruction from Location n
AS = Address of first location of Interrupt subroutine
AT = Address of Transfer Table location where new IC and BSR settings are stored

BS = Bias Register Setting
ILn = Left instruction from Location n
IRn = Right instruction from Location n
OLn = Operand for left instruction from Location n
ORn = Operand for right instruction from Location n

				PC7		PC6		PC5 = CZ						
														CAR
C1		C2		C0		C0	-	CO			C1			OCC
7	12	17 23 24 1	12	17 24	12 17 18 23 24 1	12	17 18 23 24 1	12	17 24 1 2	7	12	17 24 1		DT
														INT
														INT3
														INT1
														INT4
														INT2

No op	(None)		TRS		IL - AS	Inst. Executed
0 - No op	[n+1]	AS	BSb	[AS]	MR (n + 1, BSa)	OL - AS
0 - No op	[n+1]	AS	BSb	[AS]	[0001]	OL - AS	Memory
R	CMS[n+1]			CMS [AS]	R	R/2	R	IBR
	TRS(AT), No op			[n 1]				
S4 (AT)	ABR (n+1)	CMS(AS)	R	R	R	S4 (AR - AS)	IC
n	AT	n+1				AS	
R	R	CMS (BSb)	R	-	R	R	BSR
		BSa					
S3 (n + 1)	IC (AT)	IC(AS)	S4 (0001)	S4 (AL - AS)	S3 (AS+ 1)	ABR
A - No op	n+1	AT	AS	0001	AL - AS	
A - No op	n + 1	AT	AS	0001	AL - AS	MAR
	IC(n+1)	BSR(BSa)		0 / n + 1	0 / BSa	—	MR
						—	DT
7 12 17 23 24 1	12 17 24 1	12 13 17 18 23 24 1	12 17 18 23 24 1	12 17 24 1 2	7 12 17 24 1		DT

BS = Bias Register Setting
ILn = Left instruction from Location n
IRn = Right instruction from Location n
OLn = Operand for left instruction from Location n
ORn = Operand for right instruction from Location n

R = Full rotation of register contents
R/2 = Half rotation of register contents

INT1	S	1.11	**Interrupt Control Flip-Flops.** Used to synchronize the Interrupt state (from the 400 Cycle Counter) with the OCC and to define the intervals at the Interrupt sequence. The Interrupt sequence is inhibited (at the beginning of C1) if a long command is not in its last word time of execution or if a transfer or a JOM is to be executed in the following CO. See timing chart on preceeding page.
INT5	S	1.11	**MCUINT Storage Flip-Flop.** Remembers the MCU Interrupt signal until the Interrupt sequence can be initiated. Used in INT logic.
IO	L	3.8	**Input Odd Bit.** Presents odd bits of program selected input registers to the A Register logic.
IPU		1.0	**Instruction Processing Unit.**
ISS	S	3.5.3	**Star Scanning Mode Flip-Flop.** Set code 7311. Reset when the Scanner Servo Positioned Flip-Flop is set (SSP=1). Also reset by MOF or DOF. Used in Star Scanner logic to enable carry (SC) and borrow (SB) pulses to be generated for incrementing or decrementing the NS Register and to enable the Output Pulse Gates.
ISW	L	3.5.3	**Input SW Register.** Selects the SW Register to be read into the A Register. Used in SW Register logic to cause all register stages to be reset following readout. The star pulse width information is read into bit positions 1 through 4 of the A Register. Bit positions 5 through 24 are made zero.
ISWO	S	3.53	**Input SW Register - Odd Bits.** Holds the odd bits of the SW Register to be read into the A Register.
IUQ	I	3.1.1	**U Accelerometer Quadrature and Reference Signals.** Variable frequency
IUR	I	3.1.1	square wave input signals indicating sign and magnitude of change of velocity along the U Axis. See AUQ1, AUR1.
IUV	L	3.1.2	**Input UV Register.** Selects the UV Register to be read into the A Register. Used in UV Register logic to cause all register stages to be reset following readout. The U Accelerometer count is read into bit positions 1 through 9 of the A Register with the sign bit (position 9) extended into positions 10 through 12. The V Accelerometer count is read into bit positions 13 through 21 with the sign bit (position 21) extended into positions 22 through 24.

IVQ	I	3.1.1	V Accelerometer Quadrature and Reference Signals. See
IVR	I	3.1.1	AVQ1, AVR1.

IWD L 3.1.2 Input WD Register. Selects the WD Register to be read into the A Register. Used in WD Register logic to cause all register stages to be reset following readout. The W Accelerometer count is read into bit positions 1 through 9 of the A Register with the sign bit (position 9) extended into positions 10 through 12. The delta t count is read into bit positions 13 through 21 (sign always positive).

IWQ	I	3.1.1	W Accelerometer Quadrature and Reference Signals. See AWQ1,
IWR	I	3.1.1	AWR1.

JC	S	1.8	JOM Control Flip-Flop. Set at the beginning of DT10 if a Jump-on-Minus (JOM) command is next to be executed. Used in the X4 logic to extend the sign of the 8 bit JOM address field in forming the effective address of the jump location.
JMP	L	1.3	Jump Signal. Decoded from the Operation Code Register. Conditional on the A Register being negative ($A24=1$). Used to inhibit the AER will not change during C1 and the memory contents accessed during the following C2 will be from the JOM effective address. Therefore program control will be transferred to the JOM effective address. If JMP = 1 during C0 (right coded JOM) the AER will not change during C0 and the memory contents accessed during the following C1 will be from the JOM effective address. This has the effect of changing the operand address of the left coded instruction following a right coded JOM to the JOM effective address but does not affect program control. If the left coded instruction following a right coded JOM is a TRA, TRS or TRM, the JOM effective address will be accessed instead of the specified transfer table address, thereby giving all memory locations the capability of being used as transfer table locations.
JN	L	1.4	JOM next C0 or C1. Decoded from operation code field of IER. Used in MDTN to inhibit the Interrupt sequence. Also used in setting JC and HIS.
JOM		ı	Jump-on-Minus Command. An operation code not explicitly decoded but used in forming JMP. If the jump is executed ($A24=1$), either program control is transferred or the operand address of the following instruction is modified (see JMP). The location of the jump or operand address is relative to the Instruction Counter with a range of +127 to −128. If the jump is not executed ($A24=0$) the effect is essentially the same as if no operation had been coded.
LE	L	3.5.2	Altimeter Borrow. A 2 μs pulse occurring once for every Negative Altimeter pulse (NAL), synchronized with the Word Counter (WC1, WC2) and the digit time to occur at the proper time to decrement the Altimeter segment of the NS Register (See HBI). Used in the HBK1 and HBB1 logic.

LBT	L	2.7	Last Bit Time. A one microsecond pulse occurring every 13 us during MPY and every 12 us during all other operations. Decoded from Multiply-Divide Bit Counter (MC1-MC4). Indicates the last bit time of the 13 us multiply cycle and the 12 us divide cycle. Used in MPY to provide timing for 1) extending the sign bit of the right shifted partial product in the A Register, 2) placing the least significant bits of the partial product in the most significant end of the B Register, 3) setting up the Multiply Control Register (D1-D3) for the following cycle and 4) resetting the Carry flip-flop (CY1). Used in DIV to provide timing for 1) placing the most significant bit of the B Register (initially containing the last significant half of the dividend) into the least significant end of the A Register, 2) setting up the Divide Control flip-flop (DC) and 3) resetting the Carry flip-flop (CY1).
LC	L	3.5.2	Altimeter Carry. Same as LB for Positive Altimeter pulse (PAL). Used in the HBK1 and HBC1 logic.
LDA	L	1.3	Load Accumulator Register Command. Decoded from Operation Code Register. Used in A Register logic to allow information from specified memory location to be read into A Register.
LN1	S	3.5.2	Negative Altimeter Pulse Synchronizing Flip-Flops. Provide a single computer synchronized pulse for each negative altimeter pulse (NAL).
LN2	S	3.5.2	
LP1	S	3.5.2	Positive Altimeter Pulse Synchronizing Flip-flops. Provide a single computer synchronized pulse for each Positive Altimeter Pulse (PAL).
LRS	L	1.3	Long Right Shift Command. Decoded from Operation Code Register. Used to control gating in AU and IPU for execution of LRS command. Prior to the execution of LRS the address field of the LRS instruction (in IB13-IB18) is parallel transferred to CA1-CA6 (See CA1-CA6). During DT1 through DT12 the Control Counter is decremented at a 1 mc rate and the combined A and B Registers are shifted at 1 mc, two bits at a time, sign bit extended, until CA1 through CA5 are all zero. During DT13 through DT24 if CA6 = 1 the combined A And B Registers are rotated, bypassing the sign bit position of the B Register (B24), to accomplish the one bit right shift. With the last clock pulse of the rotation (SCF=1) the sign bit (in B1 is placed in both A24 and B24.
MA	S	2.3	M Register Odd Bit Delay Flip-Flop. Copies M1 during MPY. PC7*. Used as an additional stage in the recirculation path of the odd M Register so that the multiplicand will not precess during the 13 µs multiply cycle.
MAC	L	3.9	Manual Input Scanner Discrete Output. Code 7354.

MAGC   L   1.10   **MA Register Gated Clock.** Causes the ABR to be parallel transferred into the MAR at the middle of every DT24.

MAR   1.10   **Memory Address Register.** (MA1 - MA12)

MA1   S   1.10   **Memory Address Register.** A 12 bit parallel access register used to hold the address of the instruction or operand during the word time that the instruction or operand is being read out.

MA12   S   1.10

MB   S   2.3   **M Register Even Bit Delay Flip-flop.** Copies M2 during MPY. PC7*. Used as an additional stage in the recirculation path of the even M Register so that the multiplicand will not precess during the 13 μs multiply cycle.

MBR   L   **Modify Bias Register Command.** Decoded from the Operation Code Register. Used in the Bias Register logic to cause the Bias Register based effective address to replace the contents of the Bias Register. Modification may be in the range from +31 to -32 of the existing Bias Register contents.

MCGC   L   2.7   **MC Gated Clock.** Causes the Multiply-Divide Bit Counter to shift at 1 mc at all times other than when the counter is in the FBT state during PC7.

MCU   **Manual Control Unit**

MC1   S   2.7   **Multiply-Divide Bit Counter.**
MC2   S   2.7   A 4 stage. 1 mc serial counter
MC3   S   2.7   having 12 states during DIV. PC7*
MC4   S   2.7   and 13 states at all other times. Used to define the 12 μs add cycle during DIV and the 13 μs add cycle during MPY. Normally, the counter is free running until PC7. FBT=1. When PC7*=1 it resumes counting and if DIV=1 it skips the 0000 state.

MC1	MC2	MC3	MC4	MPY	DIV	
1	0	0	1	1	1	FBT
1	1	0	0	2	2	
0	1	1	0	3	3	
1	0	1	1	4	4	
1	1	0	1	5	5	
1	1	1	0	6	6	
0	1	1	1	7	7	
0	0	1	1	8	8	
0	0	0	1	9	9	
0	0	0	0	10		
1	0	0	0	11	10	
0	1	0	0	12	11	
0	0	1	0	13	12	LBT

MDTN	L	1.4	**Multiply, Divide, Transfer or Jump Next C0 or C1.** Decoded from IBR. Used in setting CA1 – CA3 prior to execution of MPY, DIV, TRA, TRM, TRS and JOM. Also used to inhibit the Interrupt sequence.
MGC	L	2.3	**M Register Gated Clock.** Allows the M Register to be shifted only when used. The M Register shifts at 1 mc during the add cycles of MPY and DIV and when it is used as a buffer for the Instruction Counter during the Interrupt sequence. It shifts at 250 kc while accepting operands from memory during the first word of MPY and DIV and during TRS when it is used as a buffer for the Bias Register and Instruction Counter.
MOF	I	3.9 3.5.3 3.5.4 3.6.2	**Memory Off Signal.** Generated by MCU. MOF = 1 when memory is not operational. Used to turn off certain Discrete Output and Control Flip-flops.
MPY	L	1.3	**Multiply Command.** Decoded from Operation Code Register. Used to control gating in AU and IPU for execution of Multiply command. During MPY the Operation Cycle Counter remains locked in either C0 or C1 and the Control Counter counts down to three (PC3=1) from its initial setting of 7 (PC7=1) at the word time rate. The multiplier is assumed to be in the A Register at the beginning of PC7. The multiplicand is shifted into the M Register from memory during PC7 while the multiplier is shifted into the B Register and the A Register is reset. At the end of PC7 the Multiply Control Register (D1–D3) is set up for the first add cycle. During each of the first 11 add cycles (W24=1) a new partial product is formed from the previous partial product (in the A Register) and the multiplicand and placed in the A Register, shifted two bits to the right. The two low order bits of each partial product are placed in the high order end of the B Register, replacing used multiplier bits. During the last add cycle (W25=1) the new partial product is shifted one bit to the right and becomes the final product. During the last 18 digit times of PC3 the registers are held static, with the sign bit of the product in A24 and B24, the most significant half of the product in A23 through A1 and the least significant half in B23 through B1.
MR		2.3	**M Register** (M1 – M24)
MRD	L	3.9	**MAGIC Read Discrete Output.** Code 7372
MRE	S	1.1	**Memory Read Flip-Flop – Even Bits.** Copies the even bit discriminator output at strobe clock (CPS) time.

MRO	S	1.1	**Memory Read Flip-Flop - Odd Bits.** Copies the odd bit discriminator output at strobe clock (CPS) time.
MSK	L	1.3	**Mask Command.** Decoded from Operation Code Register. Used in the A Register logic to cause the contents of the A Register to be replaced with the logical and of the A Register contents and the specified memory location contents.
M1	S	2.3	**Multiplicand - Divisor Register.** A 24 bit register used in the execution of MPY, DIV, TRS and in the Interrupt sequence. May be considered as two 12 bit shift registers with a common gated clock, one register holding the even numbered bits and the other register holding the odd numbered bits.
M24	S	2.3	
NAL	I	3.5.2	**Negative Altimeter Pulse Input.** A $75 \pm 25 \mu s$ pulse occurring each time the altimeter senses a unit change in the negative direction.
NAV	I	2.8	**Earth Navigation Mode Discrete Input.** Code 7216.
NCP	S		**Near Check Point Discrete Output Flip-flop.** Set Code 7310. Reset code 7330. Also reset by MOF.
NOD	I	3.5.2	**Negative Odometer Pulse Input.** A $75 \pm 25 \mu s$ pulse occurring each time the odometer senses a unit distance change in the backward direction.
NORMINT	I	1.11	**Normal Interrupt Signal from MCU.** Used in the INT logic to enable the computer generated interrupt.
NSGC	L	3.5.1	**NS Register Gated Clock.** Allows the NS Register to shift at 500 kc when it is being recirculated, incremented, decremented or cleared.
NSZ	S	3.5.3	**NS Register Zero Detector.** Used in the Scan Mode Control logic to set SSP when the NS Register reaches the all zeroes state during GPM or SEM.
NS1	S	3.5.1	**Earth Navigation, Star Scanner and Extrapolator Register.** A 12 stage serial shift register used as 1) an accumulator for the odometer and altimeter pulses during the Earth Navigation Mode, 2) an up-down counter for the Star Scanner Servo Control and 3) an extrapolator for generating the Sustainer Cut-off signal (SCO). The NS Register time shares Half Adder B for incrementing and decrementing. See HBI.
NS12	S	3.5.1	

OB	L	3.5.2	Odometer Borrow. A 2 μs pulse occurring once for every Negative Odometer Pulse (NOD), synchronized with the Word Counter (WC1, WC2) and the digit time to occur at the proper time to decrement the Odometer segment of the NS Register. Used in the HBK2 and HBB2 logic.
OC	L	3.5.2	Odometer Carry. Similar to OB for Positive Odometer pulse (POD). Used in HBK2 and HBC2 logic to increment the NS Register.
OCC		1.5	Operation Cycle Counter (C1, C2)
OCR		1.3	Operation Code Register (OR1-OR6)
ODT	T		Odd Digit Time. A 250 kc square wave, true in all odd numbered digit times.
ONS			Output A Register to NS Register. Used in NS Register logic to cause the 12 least significant bits of the A Register to be read into the NS Register.
ON1	S	3.5.2	Negative Odometer Pulse Synchronizing Flip-flops. Provide a single
ON2	S	3.5.2	computer synchronized pulse for each Negative Odometer Pulse (NOD).
OPU			Output Processing Unit
ORGC	L	1.3	OCR Gated Clock. Provides a clock pulse for the parallel transfer of the order code field (IB19-IB24) of the IBR to the OCR.
OR1	S	1.3	Operation Code Register. A 6 bit register used to hold the commands during execution.
OR6	S	1.3	
OTA		3.6.1	Output A Register to TA Register. Used in TA Register logic to cause the information in A1 - A7, A9 - A15 and A17 - A23 to be read into the TA Register.
OUT	L	1.3	Output Command. Decoded from the Operation Code Register. Used in the A Register logic to cause the register to recirculate.
PAL	I	3.5.2	Positive Altimeter Pulse Input. A 75 $\pm$ 25 μs pulse occurring each time the altimeter senses a unit change in the positive direction.
POD	I	3.5.2	Positive Odometer Pulse Input. A 75 $\pm$ 25 μs pulse occurring each time the odometer senses a unit distance change in the forward direction.

RDI	S	1.1	**Read Drive Inhibit Flip-flop.** Used to inhibit the memory read currents when information is not being read. Set after the first word of MPY, DIV and IDL.
RED	S	3.9	**Ready to Launch Discrete Output Flip-flop.** Set code 7312. Reset code 7332. Also reset by MOF.
RTE	L	1.3	**Rotate Command.** Decoded from Operation Code Register. Used to control gating in the AU and the IPU for execution of RTE command. Prior to the execution of RTE the address field of the RTE instruction (in IB13 - IB18) is parallel transferred to CA1 - CA6. During DT1 through DT12 the Control Counter is decremented at a 1 mc rate and the combined A and B Registers are rotated two bits at a time, by-passing the sign bit position of the B Register (B24), until CA1 through CA5 are all zero. During DT13 through DT24 if CA6 =1 the combined A and B Registers are again rotated to accomplish the one bit right shift. The sign bit of the B Register is made the same as the sign bit of the A Register.
SAC	S	3.5.3	**Sign Azimuth Coarse Flip-flop.** Set code 7301. Reset by CSR. Used in the Output Pulse Gate logic to select either CAN or CAP.
SAF	S	3.5.3	**Sign Azimuth Fine Flip-flop.** Set code 7303. Reset by CSR. Used in 1) the Output Pulse Gate logic to select either FAN or FAP, 2) the Carry and Borrow logic (SB, SC) to cause the NS Register to increment or decrement and 3) the Coarse Pulse Control (SJ1, SJ2) in selecting whether a 0 to 1 change or a 1 to 0 change in NS7 will cause a Coarse Output Pulse.
SB	L	3.5.3	**Star Scanner Borrow.** A 2 μs pulse occurring every 7.5 ms while the NS Register is non zero in 1) the Gross Positioning Mode or 2) the Star Scanning Mode if either the Azimuth or Elevation fine Eanble (EAF or EEF) has been set and the corresponding sign flip-flop (SAF or SEF) is true. The pulse is synchronized to occur at the proper word time to decrement the NS Register (See HBI). Used in HBK1 and HBB1 logic.
SBR	L	1.3	**Set Bias Register Command.** Decoded from Operation Code Register. Used in the Bias Register logic to cause the 6 most signficant bits of the Bias Register to be replaced by the address field of the SBR instruction and the 6 least significant bits replaced by zero.

SC	L	3.5.3	**Star Scanner Carry.** A 2 μs pulse occurring every 7.5 ms while the NS Register is non zero if either the Azimuth or Elevation Fine Enable (EAF or EEF) has been set and the corresponding sign flip-flop (SAF or SEF) is false. The pulse is synchronized to occur at the proper time to increment the NS Register (See HBI). Used in HKB1 and HBC1 logic.
SCF	S		**LRS and RTE Odd Bit Shift Sign Control Flip-Flop.** SCF=1 during the last half of DT24 if an add LRS or RTE is specified. Used in the A24 and B24 logic to extend the sign bit for the LRS precession.
SCO	S	3.5.4	**Sustainer Cut Off Discrete Input.** Code 7226. An internally generated signal indicating that the NS Register has reached zero in the Extrapolator Mode.
SCP	L		**LRS and RTE Precess Control.** True during DT13-24 of LRS or RTE if an odd shift is specified. Used in A and B Register Logic to cause a one bit right precession of the operand in the combined A and B Registers.
SCS	L		**LRS and RTE Shift Control.** True during DT1-12 of LRS or RTE until the rightmost 5 bits of the Control Counter (CA1-CAJ) are zero. Used in the Control Counter Logic to enable the counter to decrement and in the A and B Register Logic to cause the operand to be right shifted or rotated.
SC1	L	1.4	**Secondary Counter States.** Decoded from CA4-CA6. Used in Input-Output Addressing.
SC2	L	1.4	
SC3	L	1.4	
SC4	L	1.4	
SDP	I	3.5.3	**Star Detection Pulse.** A variable length signal from the Star Scanner indicating the presence of a star or noise. Used in the Carry Flip-flop (SHC) logic for the Pulse Width Counter and in the Scan Control Counter (SK1, SK2)
SD1	S	3.9	**Spare Discrete Output Flip-Flop No. 1.** Set code 7314. Reset code 7334. Also reset by MOF.
SE	L	1.4	**End of Short Command or End of Last Word of Long Command.** A 2 μs pulse used in effecting the parallel transfer of the instruction in IB13-IB24 to the Operation Code Register (OR1-OR6) and the Control Counter (CA1-CA6)
SEC	S	3.5.3	**Sign Elevation Coarse Flip-Flop.** Set code 7305. Reset by CSR. Used in 1) the Output Pulse Gate logic to select either FEN or FEP, 2) the Carry and Borrow logic (SB, SC) to cause the NS Register to increment or decrement and 3) the Coarse Pulse Control (SJ1, SJ2) in selecting whether a 0 to 1 change or a 1 to 0 change in NS7 will cause a Coarse Output Pulse.

SEM	S	3.5.4	Start Extrapolator Mode Flip-Flop. Set code 7350. Reset by MOF or DOF. Enables EB to decrement NS Register.
SHC	S	3.5.3	Start Pulse Width Counter Carry Flip-Flop. Produces a 2 to 8 μs signal every 7.5 ms while the Star Detection Pulse is true (SDP=1). Used in SHS to cause incrementation of the Star Pulse Width Counter.
SHS	L	3.5.3	Star Pulse Width Counter Half Adder. Used to recirculate or increment the Star Pulse Width Counter (SW1-SW4).

SJ1	S	3.5.3	**Coarse Pulse Control Flip-flops.** Used to detect a change from 0 to 1 in NS7 if the NS Register is being incremented (SAF*.SEF*=1) or a change from 1 to 0 if decremented, during the Scan Mode (ISS=1). SJ2 produces a 46 μs pulse for each such change which is directed to the Coarse Pulse Output Gates (CAP, CAN, CEP, CEN).
SK1	S	3.5.3	**Scan Control Counter.** Used to control the operation of the Star
SK2	S	3.5.3	Pulse Width Counter (SW1-SW4) and the Scan Past Counter (SP1-SP4) during the Star Scan Mode (ISS=1)

State	SK2	SK1	Operation
0	0	0	Increment SWC every 7.5 ms if SDP=1. Go to state 1 if ISS=1 and a count of 2 is in the Star Pulse Width Counter (SWC). (A count of 2 or more in the SWC is the condition for a valid star pulse.)
1	0	1	Continue incrementing SWC until SDP=0, then go to state 2.
2	1	1	Step SPC every 7.5 ms until it returns to SS7 (15 states), then go to state 3
3	1	0	Set SSP. Return to state 0.

SPC	S	3.5.3	**Scan Past Counter** (SP1-SP4)
SPGC	L	3.5.3	**Scan Past Counter Gated Clock.** Provides clock pulses for shifting the SPC every 7.5 ms (if SK2=1) or every DT6 if it is not in its initial state (SS7) and SK2=0.

SP →	4	3	2	1
SS7	0	1	1	1
SS8	0	0	1	1
SS9	0	0	0	1
SS10	0	0	0	0
SS11	1	0	0	0
SS12	0	1	0	0
SS13	1	0	1	0
SS14	0	1	0	1
SS15	0	0	1	0
SS1	1	0	0	1
SS2	1	1	0	0
SS3	0	1	1	0
SS4	1	0	1	1
SS5	1	1	0	1
SS6	1	1	1	0
SS7	0	1	1	1

SP1 S 3.5.3 Scan Past Counter. A 4 stage, 15 state Johnson
SP2 S 3.5.3 type counter used to define a 112.5 ms overshoot
SP3 S 3.5.3 past the trailing edge of the star pulse (SDP) in
SP4 S 3.5.3 the Star Scan Mode (ISS=1). Before a star is
detected the counter is initialized to state SS7.
After the fall of the star pulse it steps through the
sequence as shown, returning to SS7, and indirectly
causing the Star Scan Mode to be terminated.

SSP S 3.5.3 Scanner Servo Positioned Flip-flop. Set at the end of the scan
past the star pulse during ISS, or when the NS Register goes to
zero during GPM or SEM. Used to reset the Enable flip-flops
(EAC, EAF, EEC, EEF) and the Mode Control Flip-flops (GPM,
ISS), and in setting the EXO flip-flop.

SS7 L 3.5.3 Scan Past Counter State 7. Decoded from the SPC.

STA S 3.9 Staging Discrete Output Flip-flop. Set Code 7352. Reset by
MOF or DOF.
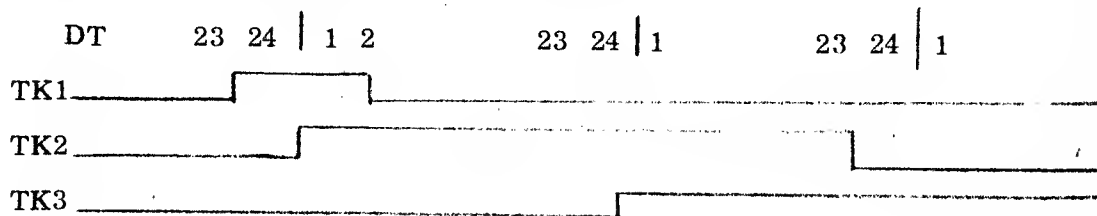
STO S 1.3 Store Command. Decoded from OCR. Used in A Register and Core
Memory logic. During STO the A Register is recirculated and
A1 and A2 go into CMO and CME.

ST1	S	3.5.3	Star Scanner Output Pulse Synchronizing Flip-flops. ST1 produces
ST2	S	3.5.3	a 46 μs pulse every 7.5 ms during GPM or ISS and is the basic timing pulse for the Star Scanner logic. ST2 prevents ST1 from being set more than once during the 7.5 ms interval.
SUB	L	1.3	Subtract Command. Decoded from OCR. Similar to ADD except that the contents of the selected memory location are subtracted from the contents of the A Register.
SWC		3.5.3	Star Pulse Width Counter. (SW1-SW4)
SW1	S	3.5.3	Star Pulse Width Counter. A four stage shift register using a unity
SW2	S	3.5.3	adder (SHS) for incrementation. Used to accumulate the number of
SW3	S	3.5.3	ST1 pulses occurring while SDP=1. The register is cleared to
SW4	S	3.5.3	zero as its contents are read out during ISW.
SZ	L	1.4	Secondary Counter State Zero. Decoded from CA4-CA6. Used in Input/Output Addressing.
S01	I	2.8	Spare Discrete Inputs.
S02			
S03			
S04			
S05			
S06			
S07			
S10			
S11	I	2.8	
S1	L	2.6	AU Odd Bit Adder. Produces the odd sum bit during ADD, SUB, MPY and DIV. Used in the A Register logic.
S2	L	2.6	AU Even Bit Adder. Produces the even sum bit during ADD, SUB, MPY and DIV. Used in the A Register logic.
S2D	S	2.6	S2 Delay Flip-flop. Delays S2 for four μs. Used in A Register logic.
S3	L	1.6	Instruction Counter Half Adder. Produces the incremented IC contents to be read into the ABR during C1.
S4	L	1.8	Operand Address Adder. Produces the effective address of the operand for the instruction to be executed during the following C0 or C1. Addresses computed during C0 go directly to the ABR. At the end of the address is parallel transferred to the AR and the contents of the effective address are accessed during C1. Addresses computed during C1 are buffered in the IC for a word time and go to the ABR during C2 to cause operand selection during C0.

TAC	L	3.9	Target Scanner Discrete Output. Code 7356.
TAGC	L	3.6.1	TA Register Gated Clock. Produces 21 clock pulses per word time for shifting the TA Register when it is being recirculated, incremented or initialized.
TAR	I	2.8	Target Data Discrete Input. Code 7270.
TA1	S	3.6.1	Gyro Torquing and Autopilot Register. A 21 stage shift register used to accept program computed output values for Gyro Torquing and Autopilot Control. During Earth Navigation and Preflight, three seven bit values corresponding to changes in the torque for three axes are sent to the TA Register and incremented or decremented at 133 kc. During flight, three seven bit values corresponding to steering error are sent to the TA Register and held until replaced.
TA21	S	3.6.1	
TB1	L	3.6.2	Gyro Torquer Borrow Pulses. Produce a 2 μs pulse every 7.5 ms, synchronized to occur at the proper time to increment a seven bit segment of the TA Register (See HBI).
TB2			
TC	S	1.8	Transfer Address Control Flip-flop. Set at the beginning of DT10 if the next command to be executed is a TRA, TRM or TRS. For these commands the rightmost 8 bits of the instruction are treated as an absolute address. Therefore TC is used to prevent X4G from turning off until the end of DT15 and to inhibit the Complement Control Flip-flop (CC) from being set.
TC1	L	3.6.2	Gyro Torquer Carry Pulses. Similar to TB1, TB2. Used to decrement a seven bit segment of the TA Register.
TC2	L		
TIM	I	2.8	Time Marker Discrete Input. Code 7272.
TK1	S	3.6.2	Gyro Torquer Control Flip-flops. Produce a control sequence every 7.5 ms. Used in the generation of the Gyro Torquer Carry and Borrow pulses and the Gyro Torquer Output Pulses.
TK2	S	3.6.2	
TK3	S	3.6.2	

DT   23 24 | 1 2   23 24 | 1   23 24 | 1

TK1

TK2

TK3

TNX	S	3.6.2	**Gyro Torquer Inhibit Flip-flops.** Detect zero in each of the three
TNY	S	3.6.2	seven bit segments of the TA Register corresponding to the X, Y
TNZ	S	3.6.2	and Z axes. Used to inhibit the corresponding Carry, Borrow and Output Pulses.
TPG	L	3.6.2	**Torquer Pulse Gate.** A state of the Control Flip-flops (TK2-TK3) used in the Gyro Torquer Output Pulse Gates.
TRA	L	1.3	**Transfer Absolute Command.** Decoded from OCR. Used in IPU logic. Prior to execution of TRA the Control Counter (CA1-CA3) is initialized to PC7. During the three word times required for TRA it counts down to PC5. During PC7 the contents of the Transfer Table location specified in the 8 bit address part of the instruction replace the contents of the Bias Register and the Instruction Counter, and the ABR accepts the new Instruction Counter setting. During PC6 the instruction pair in the first transfer location is read into the IBR and during PC5 the effective address of the operand for the left hand instruction is computed.
TRM	L	1.3	**Transfer on Minus Command.** Decoded from the IBR and the sign bit of the A Register (A24). TRM is used to force the OCR to the TRA state if the sign of A is negative (A24=1). If A24=0, no command is executed.
TRS	L	1.3	**Transfer to Subroutine Command.** Decoded from OCR. Used in IPU logic. Same as TRA with the following exceptions: 1) During PC7 the contents of the Bias Register and the Instruction Counter are sent to the M Register 2) During PC6 the ABR is cleared to zero 3) During PC5 the contents of the M Register are stored in location zero. If TRS is left coded in location n, the unincremented IC(n) will be stored. If TRS is right coded, the incremented IC (n+1) will be stored.
TSA	I	2.8	**Target Selection Discrete Inputs.** Codes 7274 and 7276.
TSB	I	2.8	
TSX	S	3.6.2	**Gyro Torquing Polarity Control.** Detect the sign bits of each of the
TSY	S	3.6.2	three seven bit segments of the TA Register corresponding to the X,
TSZ	S	3.6.2	Y and Z axes. Used in Carry/Borrow selection, Output Pulse selection and zero detection.
TXN	L	3.6.2	**Gyro Torquing Output Pulse Gates.** Produce 46 μs pulses every 7.5 ms
TXP			when the corresponding Inhibit Flip-flops are false. Negative (N) and
TYN			positive (P) pulses are mutually exclusive for each axis.
TYP			
TZN			
TZP	L	3.6.2	

UQ	I	3.1.1	U Axis Accelerometer Quadrature Signal Input. See AUB.
UR	I	3.1.1	U Axis Accelerometer Reference Signal Input. See AUB.
UVGC	L	3.1.2	UV Register Gated Clock. Produces two groups of nine 1 mc clock pulses for recirculation and incrementation and two groups of nine 500 kc clock pulses for readout to the A Register.
UV1	S	3.1.2	UV Register. An 18 bit shift register used to accumulate pulse counts for the U and V axis accelerometers. The UV Register is addressable as an input to the A Register and is cleared to zero
UV18	S	3.1.2	on readout.
VQ	I	3.1.1	V Axis Accelerometer Quadrature Signal Input. See AUB.
VR	I	3.1.1	V Axis Accelerometer Reference Signal Input. See AUB.
WC1	S	3.2	Word Counter. A two stage, four state binary counter providing
WC2	S	3.2	timing signals for 1) control of time sharing of Half Adder B and 2) synchroniztion of input signals.

DT   24   1   24   1   24   1   24   1   24   1

WC1P

WC1

WC2P

WC2
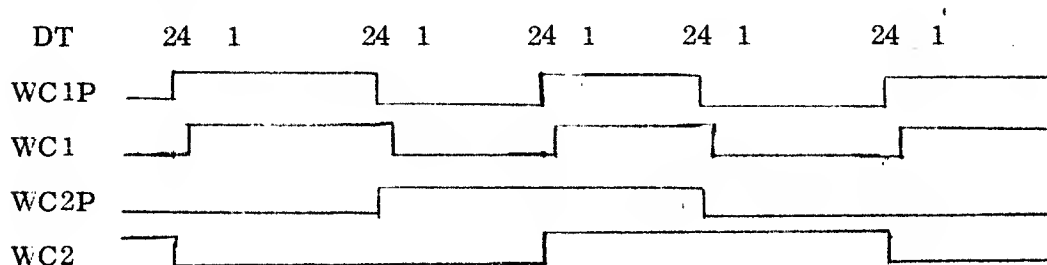
WDGC	L	3.1.2	WD Register Gated Clock. Produces two groups of nine 1 mc clock pulses for recirculation and incrementation and two groups of nine 500 kc clock pulses for readout to the A Register.
WDSTEP	I	1.13	Word Step Signal from MCU.
WDI	S	1.1	Write Drive Inhibit. Copies RDI at DT1. Used to inhibit write currents during MPY, DIV and IDL.
WD1	S	3.1.2	WD Register. An 18 bit shift register used to accumulate pulse counts for the W axis accelerometer and real time. The WD Register is addressable as an input to the A Register and is cleared to zero
WD18	S	3.1.2	on readout.

WQ	I	3.1.1	W Axis Accelerometer Quadrature Signal Input. See AUB.
WR	I	3.1.1	W Axis Accelerometer Reference Signal Input. See AUB.
WS	S	1.13	WDSTEP Sync. Flip-flop. Synchronizes the WDSTEP signal from the MCU with the computer word time. Used in IDL logic to enable one operation cycle and return to C2.
W24	S	2.4	Words 2 through 4 of MPY. Set at the beginning of the second word of MPY (PC6) and reset at the end of the 11th add/subtract cycle. Used in A, B and M Register logic to control clocks and inputs.
W25	S	2.4	Last cycle of MPY. True during the last 13 μs add/subtract cycle of MPY. Used in A, B, and M Register logic to control clocks and inputs.
W27	S	2.5	Words 2 through 7 of DIV. Set at the beginning of the second word of DIV (PC6) and reset at the beginning of the 8th word (CZ=1). Used in A, B, and M Register logic to control clocks and inputs.
XAB	L	1.3	Exchange A and B Registers Command. Decoded from OCR. Used in A and B Register logic. During XAB the contents of the A Register are replaced with the contents of the B Register and vice versa.
X1	L	2.6	Odd Bit Adder Augend Input. Presents the odd bit of the augend to the Odd Bit Adder (S1). During DIV the one bit left shifted contents of the A Register is the augend input. For the Odd Bit Adder this data appears in AB. During MPY. LBT the sign of the contents of the A Register is extended. This data also appears in AB. During MPY. LBT*, ADD and SUB, A1 is the odd augend input.
X2	L	2.6	Even Bit Adder Augend Input. Presents the even bit of the augend to the Even Bit Adder (S2). The one bit left shifted A Register contents appears in A1 during DIV and the extended sign bit appears in AB during MPY. LBT. During MPY. LBT*, ADD and SUB, A2 is the even augend input.
X4	L	1.8	Operand Address Adder Addend Input. Presents the address field of the next command to be executed to the Operand Address Adder. Also presents "1" bits for extending the sign or for producing a 77_8 or 76_8 in the 2 MSD's of the address for absolute addressing.
X4G	S	1.8	X4 Gate Flip-flop. Used to inhibit X4 during DT15 if the next command is not a transfer and does not refer to working storage ($77XX_8$ or $76XX_8$).

Y1	L	2.6	Odd Bit Adder Addend Input. Presents the odd bit of the addend to the Odd Bit Adder (S1). During MPY. LBT* either the multiplicand (if D1=1) or the one bit left shifted multiplicand (if D2=1) is the addend input. For the Odd Bit Adder this data appears in either M1 or MB. During DIV the divisor is the addend input and appears in M1. During ADD and SUB, MRO is the addend input.
Y2	L	2.6	Even Bit Adder Addend Input. Presents the even bit of the addend to the Even Bit Adder (S2). During MPY. LBT* this data appears in M2 (if D1=1) or in M1 (if D2=1). During DIV the divisor data appears in M2. During ADD and SUB, MRE is the addend input.
Y4	L	1.8	Operand Address Adder Augend Input. Presents the contents of either the Bias Register (BSR) or the Instruction Counter (IC) as the basis of the effective address of the operand for the next command to be executed.
Y4G	S	1.8	Y4 Gate Flip-Flop. Used to enable Y4 if the next command is a core reference command or a JOM.